MIMOSA26
User Manual

(Preliminary version)

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MIMOSA26 chip			
Version	Date	Description	Comments
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MIMOSA26

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1 Introduction

1.1 General description of EUDET CMOS pixel sensor

MIMOSA26 is the final sensor chip of EUDET JRA1 beam telescope for the ILC vertex detector studies. Its architecture is based on the MIMOSA22 (Monolithic Active Pixel Sensor (MAPS) with fast binary readout) and on a prototype circuit named SUZE01 which performs integrated zero suppression. The size of the chip is 13,7 mm x 21,5 mm and the sensor matrix is composed by 576x1152 pixels of 18.4 µm pitch. The pixel design is based on self biased diode radtol architecture. The design process is Austria Mikrosysteme AMS-C35B4/OPTO which uses 4 metal- and 2 poly-layers. The thickness of the epitaxial layer is 14 µm. The design tools are CADENCE DFII 5.1 with DIVA, ASSURA, CALIBRE rules. The chip has been submitted in an Engineering Run via CMP on 19th December 2008.

In the EUDET beam telescope, the hit rate is less than 5 hits/ image. However, MIMOSA26 is suited for charged particles detecting with density up to 10^6 hits /cm²/s. The design of the sensor is driven by the high readout frequency in order to keep the track multiplicity per frame at a low level. It is done by read out pixel columns in parallel, row by row. The chip readout time is 115.2 µs. Each pixel includes an amplification and Correlated Double Sampling (CDS) and each end of column is equipped with a discriminator. After analogue to digital conversion, digital signals pass through the zero suppression circuits. The digital signals are processed in parallel on 18 banks, then arranged and stored in a memory row by row. Two memories banks have been implemented in the sensor to perform read and write operations simultaneously (see Figure 1 : MIMOSA26 functional view).

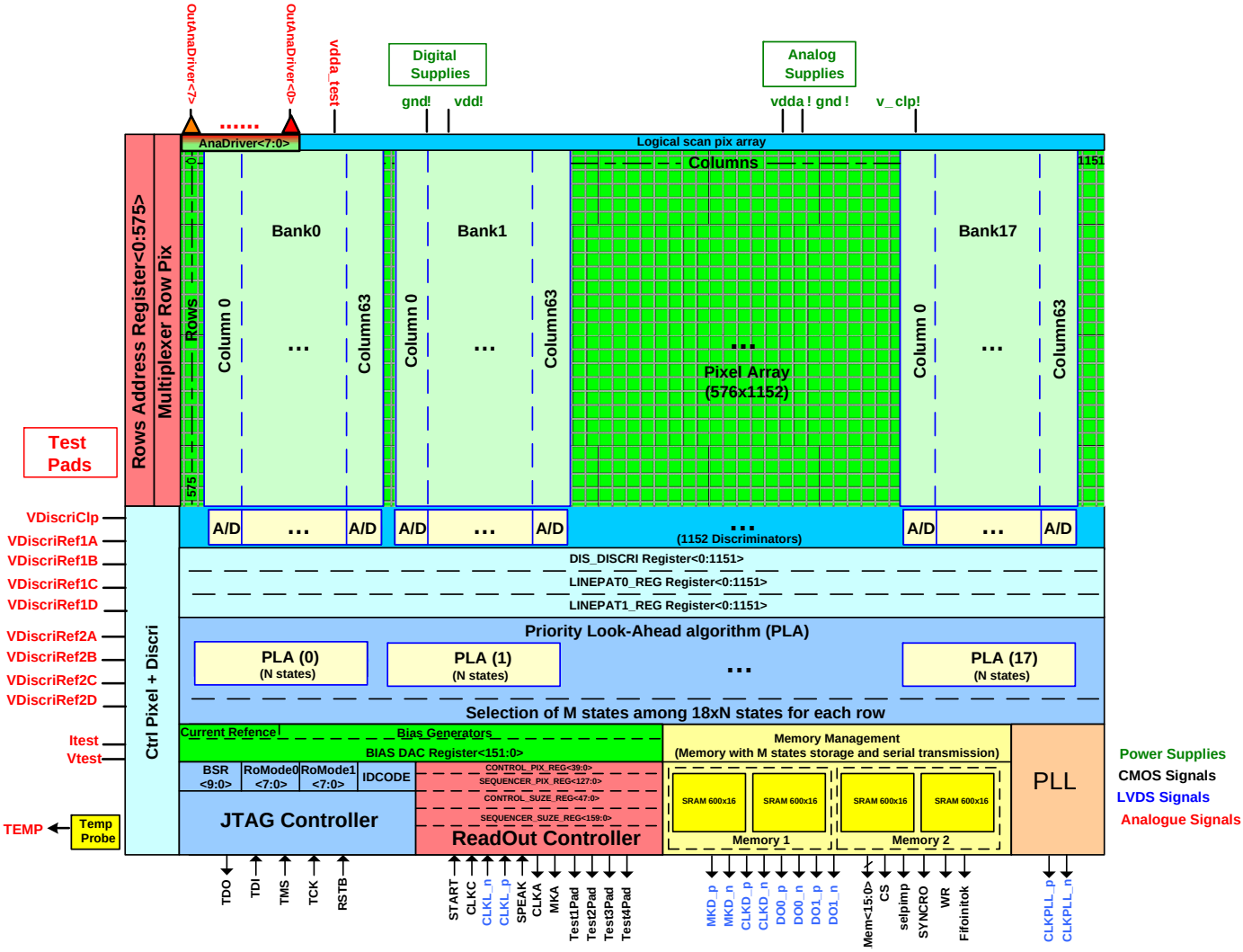


Figure 1 : MIMOSA26 functional view
Does not correspond to the floorplan neither for the core, neither for the pad ring

1.2 DIGITAL PART (SUZE)

The following synoptic shows the implementation of SUZE into MIMOSA 26.

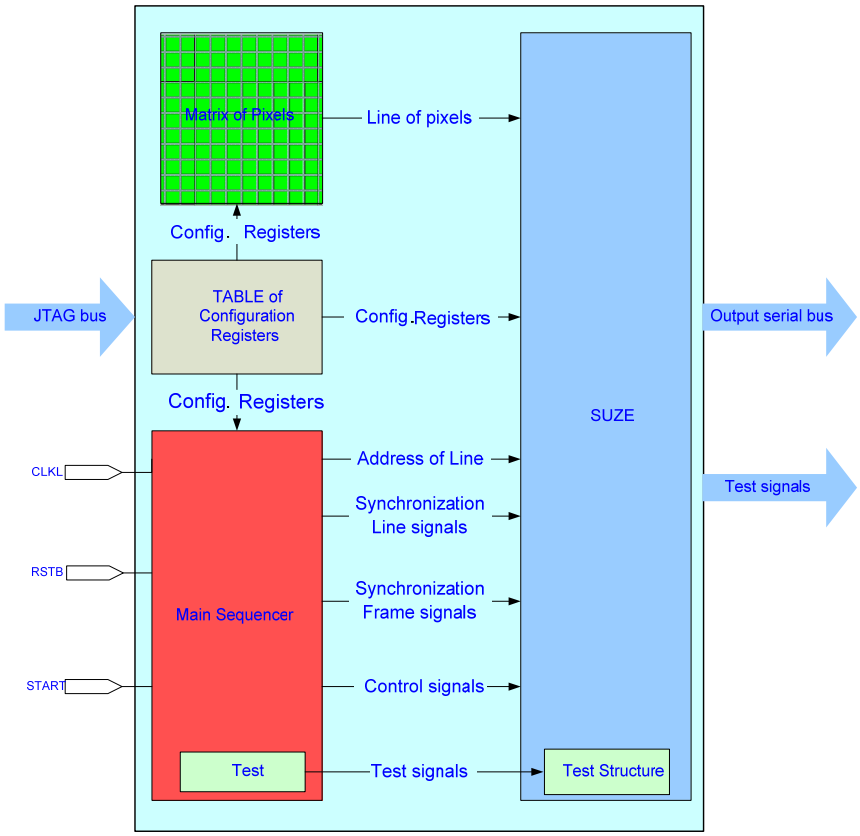


Figure 2: top view implementation of SUZE in MIMOSA 26

This digital part manages sequentially each line for the whole frame composed of 576 lines of 1152 columns. The main sequencer gives to the structure the address of lines and all synchronisations and controls signals. A JTAG controller brings the configuration information. (Table of configurations registers) A test structure simulates a matrix of pixel in order to check the functions of SUZE. These debugging tests are reserved for the IPHC/IRFU group.

2 Control Interface

2.1 Introduction

The control interface of MIMOSA26 complies with Boundary Scan, JTAG, IEEE 1149.1 Rev1999 standard. It allows the access to the internal registers of the chip like the bias Register and the different registers control.

On Power-On -Reset, an internal reset for the control interface is generated. The finite state machine of the Test Access Port (TAP) of the controller enters in the Test-Logic-Reset state and the ID register is selected.

MIMOSA26 has been designed in order to be fully adjustable via the control interface. Nevertheless several voltages level can be set either via the control interface or via a pad.

2.2 JTAG Instruction Set

The Instruction Register of the JTAG controller is loaded with the code of the desired operation to perform or with the code of the desired data register to access.

Instruction	5 Bit Code$_{16}$	Selected Register	Notes
EXTEST	01	BSR	JTAG mandatory instruction
HIGHZ	02	BYPASS	JTAG mandatory instruction
INTEST	03	BSR	JTAG mandatory instruction
CLAMP	04	BYPASS	JTAG mandatory instruction
SAMPLE_PRELOAD	05	BSR	JTAG mandatory instruction
ID_CODE	0E	DEV_ID register	User instruction
BIAS_GEN	0F	BIAS_DAC	DATAREG0
LINE0_PATTERN_REG	10	LINE0PAT_REG	DATAREG1
DIS_DISCRI	11	DIS_DISCRI	DATAREG2
SEQ_PIX_REG	12	SEQUENCER_PIX_REG	DATAREG3
CTRL_PIX_REG	13	CONTROLER_PIX_REG	DATAREG4
LINE1_PATTERN_REG	14	LINE1PAT_REG	DATAREG5
SEQ_SUZE_REG	15	SEQUENCER_SUZE_REG	DATAREG6
HEADER_TRAILER_REG	16	HEADER_REG	DATAREG7
CTRL_SUZE_REG	17	CONTROLER_SUZE_REG	DATAREG8
CTRL_8b10b_REG0	18	CONTROLER_8b10b_REG0	DATAREG9
CTRL_8b10b_REG1	19	CONTROLER_8b10b_REG1	DATAREG10
NU1	1A		DATAREG11
NU2	1B		DATAREG12
NU3	1C		DATAREG13
RO_MODE1	1D	ReadOut Mode 1	DATAREG14
RO_MODE0	1E	ReadOut Mode 0	DATAREG15
BYPASS	1F	BYPASS	JTAG mandatory instruction

(1) Instruction codes implemented but not the corresponding registers. To be fixed in the next version.

2.3 JTAG Register Set

JTAG registers are implemented with a Capture/Shift register and an Update register. JTAG standard imposes that the last significant bit of a register is downloaded/shifted first.

Register Name	Size	Access	Notes
INSTRUCTION REG	5	R/W	Instruction Register
DEV_ID	32	R Only	
BSR	10	R/W	Boundary scan register
BIAS_DAC	152	R/W	Previous value shifted out during write
LINE0PAT_REG	1152	R/W	Previous value shifted out during write
DIS_DISCRI	1152	R/W	Previous value shifted out during write
SEQUENCER_PIX_REG	128	R/W	Previous value shifted out during write
CONTROLER_PIX_REG	40	R/W	Previous value shifted out during write
LINE1PAT_REG	1152	R/W	Previous value shifted out during write
SEQUENCER_SUZE_REG	160	R/W	Previous value shifted out during write
HEADER_REG	64	R/W	Previous value shifted out during write
CONTROLER_SUZE_REG	48	R/W	Previous value shifted out during write
CONTROLER_8b10b_REG0	144	R/W	Previous value shifted out during write
CONTROLER_8b10b_REG1	312	R Only	
NU1…..NU3	0		Not implemented. For future use
RO_MODE1	8	R/W	Previous value shifted out during write
RO_MODE0	8	R/W	Previous value shifted out during write
BYPASS	1	R Only	

2.3.1 Instruction Register

The Instruction register is a part of the Test Access Port Controller defined by the IEEE 1149.1 standard. The Instruction register of MIMOSA26 is 5 bits long. On reset, it is set with the ID_CODE instruction. When it is read the 2 last significant bits are set with the markers specified by the standard, the remaining bits contain the current instruction.

X	**X**	**X**	**1**	**0**

2.3.2 DEV_ID Register

The Device Identification register is implemented. It is 32 bits long and has fixed value hardwired into the chip. When selected by the ID_CODE instruction or after the fixed value is shifted via TDO, the JTAG serial output of the chip. MIMOSA26 ID_CODE register value is M26 + *0x4D323601*.

Bit #	Bit Name	Purpose	Default value $Code_{16}$		
31-0	ID_CODE	Device Identification register	4D323601	*ASCII*	*HEX*
				‘M’	4D
				‘2’	32
				‘6’	36
				<SOH>	01

2.3.3 Boundary Scan Register

The Boundary Scan Register, according with the Jtag instructions, tests and set the IO pads.
The MIMOSA26 BSR is 10 bits long and allows the test of the following input and outputs pads.

Bit #	Corresponding Pad	Type	Signal	Notes
9	SPEAK	Input	SPEAK	Active Readout Marker & Clock
8	CLKC	Input	CkCMOS	CMOS Clock
7	START	Input	START	Readout : Input synchronisation
6	LVDS CLKL_n/CLKP_p	Input	ClkLvds	Resulting CMOS signal after LVDS Receiver
5	No Used			
4	No Used			
3	No Used			
2	CLKA	Ouput	CLKA	Readout Analogue Clock
1	Test2Pad	Ouput	Tst2Pad	Readout Test Pad 2
0	Test1Pad	Ouput	Tst1Pad	Readout Test Pad 1

2.3.4 BIAS_DAC Register

The BIAS_DAC register is 152 bit wide; it sets simultaneously the 19 DAC registers.
As show bellow these 8-bit DACs set voltage and current bias. After reset the register is set to 0, a value which fixes the minimum power consumption of the circuit. The current values of the DACs are read while the new values are downloaded during the access to the register. An image of the value of each DAC can be measured on its corresponding test pad.

Bit range	DAC #	DAC Internal Name	DAC purpose	Corresponding Test Pad
151-144	DAC18	IKIMO	External circuit monitoring	Vtest
143-136	DAC17	IPIX	Pixel source follower bias	IPIX
135-128	DAC16	IDIS2	Discriminator bias 2	IDIS2
127-120	DAC15	IDIS1	Discriminator bias 1	IDIS1
119-105	DAC14	IVDREF2	Discriminator Reference 2	VDREF2
111-104	DAC13	IVDREF1A	Discriminator Reference 1 (Bank A)	VDREF1A
103-96	DAC12	IVDREF1B	Discriminator Reference 1 (Bank B)	VDREF1B
95-88	DAC11	IVDREF1C	Discriminator Reference 1 (Bank C)	VDREF1C
87-73	DAC10	IVDREF1D	Discriminator Reference 1 (Bank D)	VDREF1D
79-72	DAC9	IAnaBUF	Analogue Buffer bias	IAnaBUF
71-64	DAC8	IVTST2	Test Level, emulates a pixel output	
63-56	DAC7	IVTST1	IDEM	
55-48	DAC6	ILVDS	LVDS PAD bias	ILVDS
47-40	DAC5	ILVDSTX	LVDS PAD bias	ILVDSTX
39-32	DAC4	ID2PWRS	Discriminator bias 2 (mode low consp.)	
31-24	DAC3	ID1PWRS	Discriminator bias 1 (mode low consp.)	
23-16	DAC2	IBufBias	Ref&Tst Buffer bias	BUFBIAS
15-8	DAC1	IPwrSWBias	Discriminator Power Pulse bias	PWRSWBIAS
7-0	DAC0	ICLPDISC	Discriminator Clamping bias	DISCLP

2.3.5 LINEPAT0_REG Register

The LINEPAT0_REG register is 1152 bits large. The purpose of this register is to emulate discriminators outputs rows in *En_LineMarker* and Pattern_Only modes.

When *Pattern_Only* is active, the values stored in the pixel matrix are ignored and the value of LINEPAT0_REG is sent to the output. This is a test mode which emulates the (digital) pixel response with the contents programmed into the LINEPAT0_REG register in order to verify the digital processing. The pattern is alternated with the contents of the LINEPAT1_REG.

In the *En_LineMarker* mode, it adds two rows at the end of matrix for a readout chip and the LINEPATL0_REG register is read to emulate the discriminators outputs of these two supplementary rows.

After the initialisation phase (reset), this register is preset to 0.

Bit #	Bit Name	Purpose	Basic configuration value $Code_{16}$
0-1151	LinePatL0Reg	Emulate discriminators rows	AAAAAA_AAAAAAAA_AAAAAAAA_AAAAAA AA(1)

(1) Example of pattern used in simulation.

In MIMOSA26, the LinePatL0Reg <0> is on the left hand side while LinePatL0Reg <1151> is on the right hand side.

2.3.6 DIS_DISCRI Register

The DIS_DISCRI register is 1152 bits large. The purpose of this register is to disable the discriminator on a specific column if it is noisy, by gating Latch signal and setting the output discriminator at 0.

The default value of the DIS_DISCRI register is 0; it means that all discriminators are activated. Setting a bit to 1 disables the corresponding discriminator. In MIMOSA26, the DisableLatch<0> is on the left hand side while DisableLatch<1151> is on the right hand side.

0 (Lsb)	**1151 (Msb)**
DisableLatch<0>	**DisableLatch<1151>**

2.3.7 SEQUENCER_PIX_REG Register

The SEQUENCER_PIX_REG registers are 128 bits large; this register contains all parameters to generate readout pixel and discriminator sequence.

Bit #	Bit Name	Purpose	Basic configuration value $Code_{16}$	Signal Name
127-112	DataRdPix	Connect pixel output to common column	FFFF	Slct_Row_Int
111-96	DataRst1	Set reference voltage for diode	0040	Rst
95-80	DataClp	Set reference voltage for clamping	01C0	Clamp
79-64	DataCalib	Sample after clamping	3C00	Calib
63-48	DataRdDsc	Sample before clamping	001C	Read
47-32	DataLatch	Latch state of the discriminator	6000 (1)	Latch
31-0	DataPwrOn	Activate power supply for pixel	FFFFFFFF	Pwr_On

Example: Generation of Latch Signal

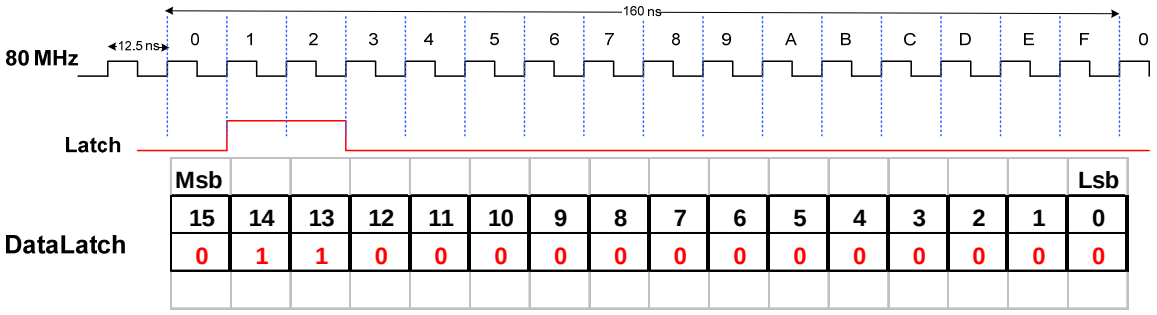


Figure 3 : Example: Generation of Latch Signal

- Related timing with f_{clk}=80 MHz (Read, Calib, Latch signals are used by the column readout circuitry).

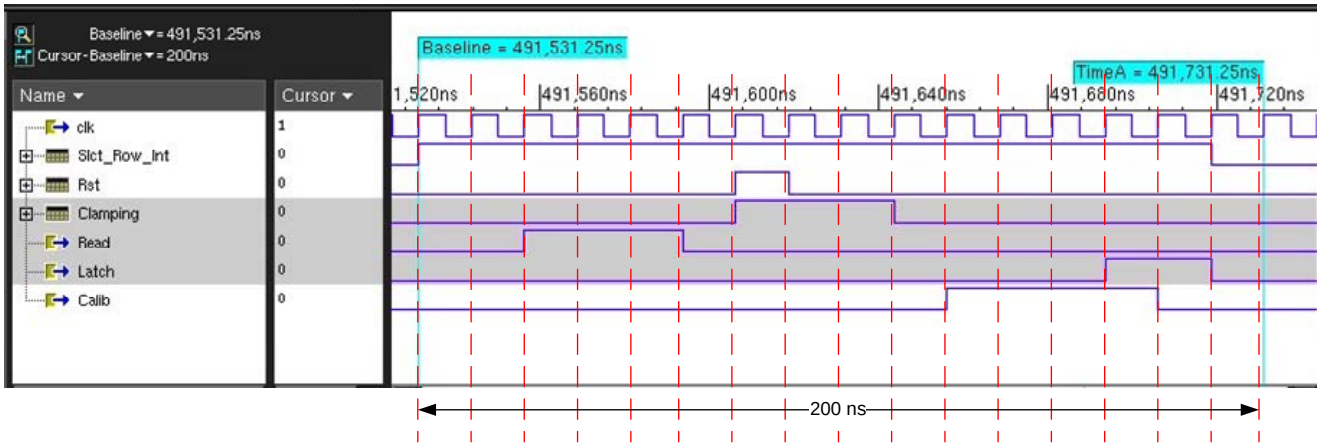


Figure 4 : Simulation timing diagram for signals of SEQUENCER_PIX_REG (1)

- This is readout sequence of the pixel and discriminator for 2 successive rows of matrix. In the waveform, the indexation of internal signal vectors is reversed compared with the MIMOSA26 functional view (for example, the signal Pwr_On[575] corresponds to the row at the top of matrix).

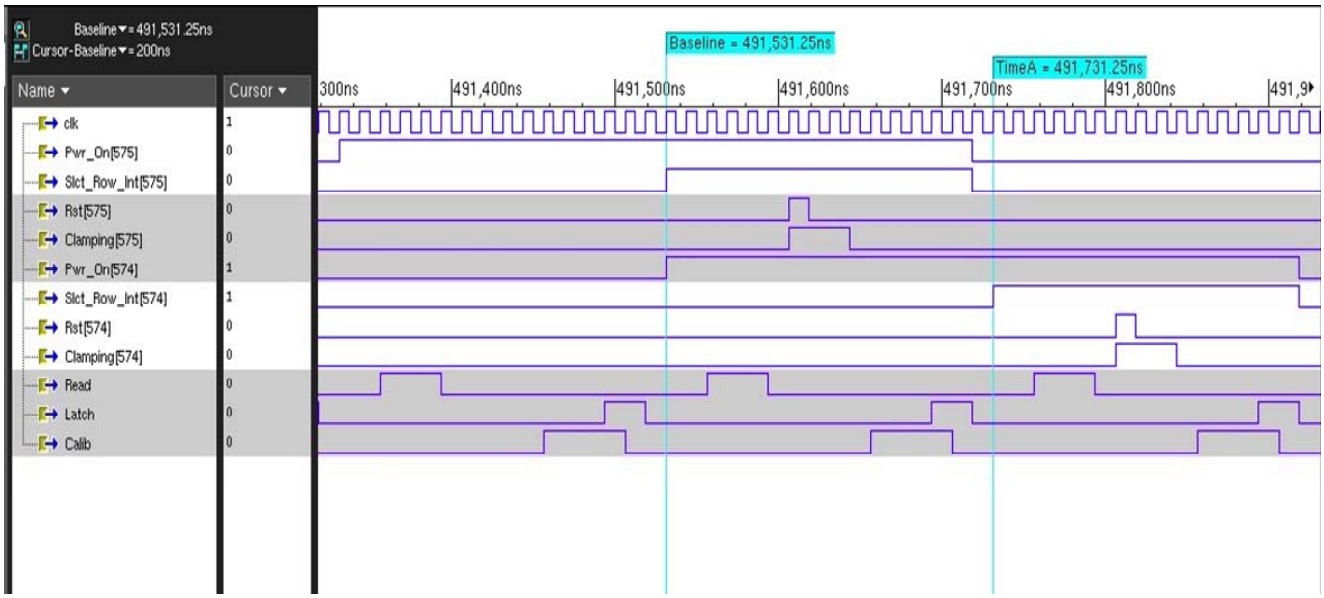


Figure 5 : Simulation timing diagram for signals of SEQUENCER_PIX_REG (2)

2.3.8 CONTROL_PIX_REG Register

The CONTROL_PIX_REG registers are 40 bits large; they allow setting parameters of the readout controller. These registers are reserved for sensor's debugging by the IPHC/IRFU group. A end user has to respect to the default values.

Bit #	Bit Name	Purpose	Basic configuration value $Code_{16}$	
39-36	NU	Reserved, Not Used	0	
35-33	SelPad1	Selection bit of Test1Pad	0	MK_Test_A signal
32-30	SelPad2	Selection bit of Test2Pad	0	MK_Test_D signal
29-20	RowMkLast	Row number of the frame. It depends of readout mode. When the En_HalfMatrx mode is active, the value is 0x013F otherwise 0x023F. When the En_LineMarker mode is active, add two rows at the end of matrix.	023F	Normal mode, the number of row matrix is 576.
19-10	RowMkd	Selection parameter of row for digital marker (MK_Test_D)	0	Digital marker place is first row of matrix during the readout
9-0	RowMka	Selection parameter of row for analogue marker (MK_Test_A)	0	analogue marker place is first row of matrix during the readout

2.3.9 LINEPAT1_REG Register

The LINEPAT1_REG register is 1152 bits large. The purpose of this register is to emulate discriminators outputs rows in *En_LineMarker* and Pattern_Only modes.

When *Pattern_Only* is active, the values stored in the pixel matrix are ignored and the value of LINEPAT1_REG is sent to the output. This is a test mode which emulates the (digital) pixel response with the contents programmed into the LINEPAT0_REG register in order to verify the digital processing. The pattern is alternated with the contents of the LINEPAT1_REG.

In the *En_LineMarker* mode, it adds two rows at the end of matrix for a readout chip and the LINEPATL1_REG register is read to emulate the discriminators outputs of these two supplementary rows.

Bit #	Bit Name	Purpose	Basic configuration value $Code_{16}$
0-1151	LinePatL1Reg	Emulate discriminators rows	555555_55555555_55555555_55555555(1)

(1) Example of pattern used in simulation.

In MIMOSA26, the LinePatL1Reg <0> is on the left hand side while LinePatL1Reg <1151> is on the right hand side.

With Line1_PAT_REG together these two signals will form the elements of the simulated frame given to SUZE part.

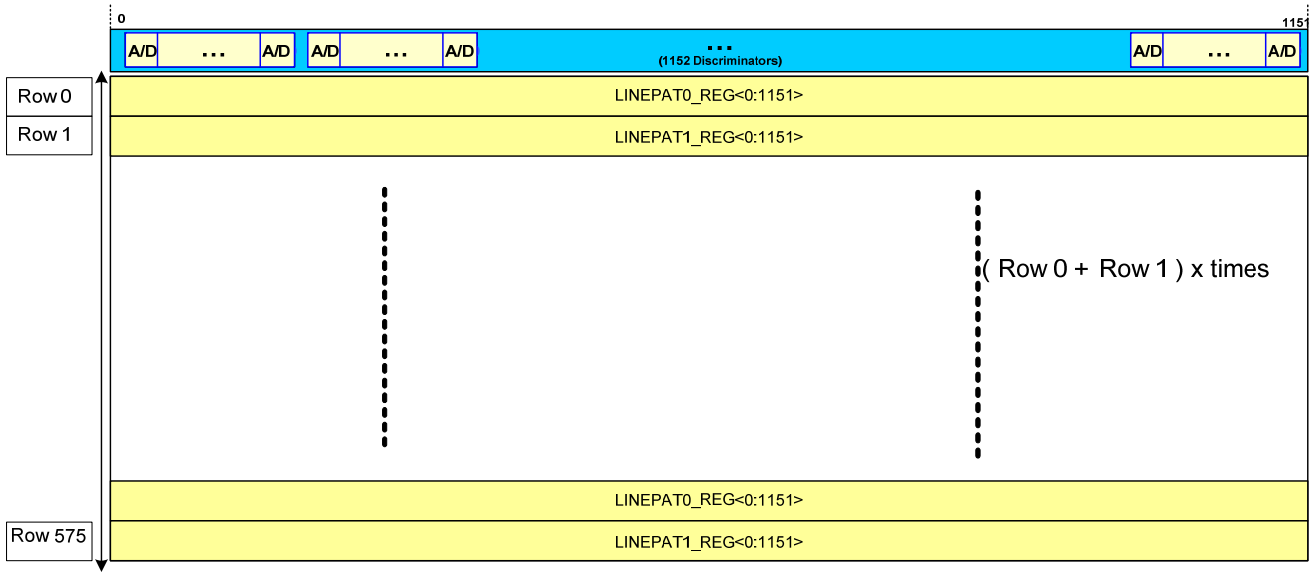


Figure 6 : Generation of the test frame pattern

2.3.10 SEQUENCER_SUZE_REG

The SEQUENCER_SUZE_REG registers are 160 bits large; this register contains all parameters to generate readout zero suppression (SUZE) sequence.

Bit #	Bit Name	Purpose	Basic configuration value $Code_{16}$	Signal Name
159-144	dckreadpixmux	Sample signal for multiplexer after Priority look ahead	0555	CkReadPixMux
143-128	dcklatchhit	Synchronization signal every line for Priority Look Ahead	3000	CkLatch
127-112	dcklatchhitmem	Synchronization signal every line for memory management	1000	CkLatchMem
111-96	dckmemlatch	Synchronization signal every line for Priority Look Ahead	0555	CkMemLatch
95-80	dckreadpix5ns	Synchronization signal 6 times every line for memory management shifted of 5 ns compared with CkReadpix	82aa	CkReadPix5ns
79-64	dckreadpix	Synchronization signal 6 times every line for memory management	0555	CkReadPix
63-48	dstartingline	Synchronization signal every line for memory management	e001	debutligne
47-32	drstline	Synchronization signal every line for all SUZE part	6000	RstLine
31-16	drstpix	Reset signal 6 times every line for Priority Look Ahead	0555	RstPix
15-0	drstframe	Reset frame signal for memory management	2000	RstTrame

- Related timing with f_{clk}=80 MHz (Theses signals are used by zero suppression circuit).

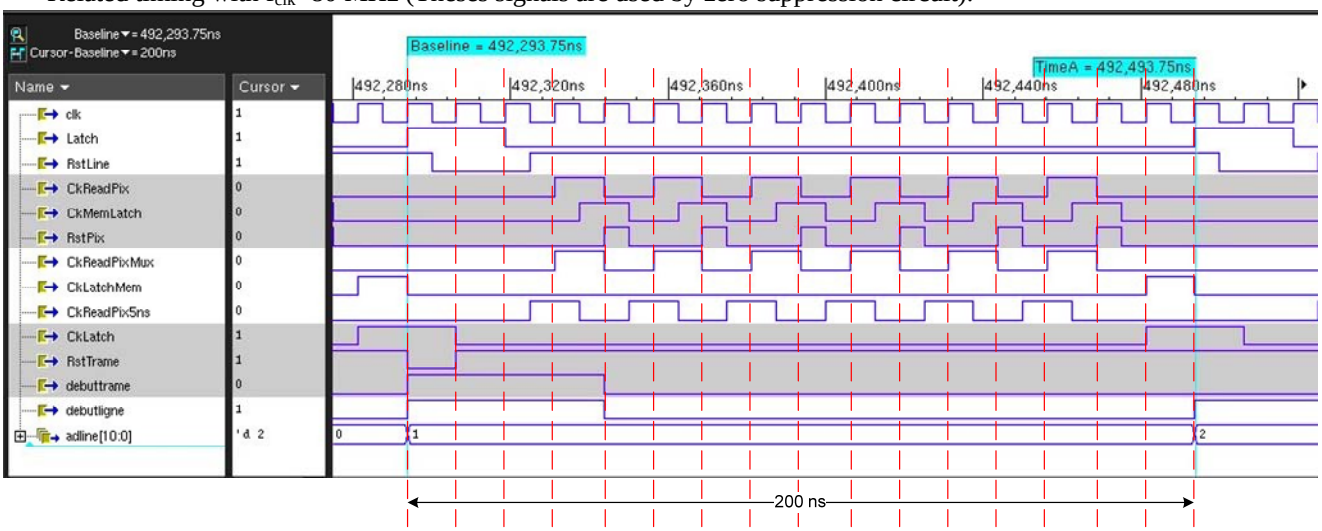


Figure 7 : Simulation timing diagram for signals of SEQUENCER_SUZE_REG

2.3.11 HEADER_REG

The register called Header_Reg includes 4 registers of 16 bits as shown below.

Bit #	Bit Name	Purpose	Basic configuration value	
63-48	header0	Synchronisation header for serial output0	5555	
47-32	header1	Synchronisation header for serial output1	5555	
31-16	trailer0	Synchronisation trailer serial output0	AAAA	
15-0	trailer1	Synchronisation trailer serial output1	AAAA	

For both modes according to the register DUALCHANNEL the header and the trailer of each data frame can be different. The following table shows the possible *Header* and the *Trailer* which ensure the unicity in the data frame. The unicity is guaranteed without the *Frame counter*.

Bits	0-3 (in hexa)	4-14	15
Possible Header or Trailer	1	X	1
	2	X	1
	3	X	1
	4	X	1
	5	X	1
	6	X	1
	7	X	1
	8	X	1
	A	X	1
	B	X	1
	C	X	1
	D	X	1
	E	X	1
	F	X	1

Table 1: possible *Header* and *Trailer* for mode 0 and 1 to ensure unicity (or mode 2 with 32 bits)

2.3.12 CONTROL_SUZE_REG Register

The CONTROL_SUZE_REG registers are 48 bits large; they allow setting parameters of the readout controller for SUZE. We suggest an end user to only use default values except for data stream output parameters

Bit #	Bit Name	Purpose	Basic configuration value Code$_{16}$	
47-46	NU	Reserved, Not Used	0	
45-43	SelPad4	Selection bit of Test4Pad	0	debutligne
42-40	SelPad3	Selection bit of Test3Pad	0	cklatchhit
39	En_auto_scan_discri	Enable mode scan test discriminators, all matrix	0	Debugging reserved for IPHC Cf. §3.5.2.2
38	En_scan	Enable mode scan test	0	Debugging reserved for IPHC Cf. §3.5.2.2
37	Test_after_mux	Enable mode scan test for multiplexer of SUZE	0	Debugging reserved for IPHC
36	entestdatadisc	Enable mode scan test discriminators	0	Debugging reserved for IPHC Cf. §3.5.2.2
35-26	RowLastSuze	Row number of the frame. It depends of readout mode. When the En_HalfMatrx mode is active, the value is 0x013F otherwise 0x023F. When the En_LineMarker mode is active, add two rows at the end of matrix.	023F	Normal mode, the number of row matrix is 576.
25-16	ScanLineTst	Selection parameter of row for digital	0	Digital marker place is first row of matrix during the readout
15	dualchannelout	Determines the data stream on the channel or in one channel	0	Cf. explanation of the data stream output
14	clkrateout	Determines the clock rate of the outputs channel or in one channel	0	Cf. explanation of the data stream output
13	jsupinitmem	Authorizes the initialization test of the FIFO or not. High level active.	1	
12	disckgmodgate	Discriminator switched ON/Off	0	
11-9	cfgwr	Cf. cfg multiplexors configuration	0	
8-6	cfgdata	Idem	0	
5-3	cfgcs	Idem	0	
2-0	cfgadr	Idem	0	

The internal following signals can be selected with SelPad3 and SelPad4 bits.

SelPad3	Tst3Pad	Purpose	SelPad4	Tst4Pad	Purpose
0	cklatchhit	Cf; sequencer_SUZE_reg	0	debutligne	
1	cklatchhitmem	“ “	1	rstline	
2	ckmemlatch	“ “	2	debuttrame	
3	ckreadpix	“ “	3	rsttrame	
4	ckreadpix5ns	“ “	4	rst_frame	
5	ckreadpixmux	“ “	5	rstpix	
6	latch	“ “	6	synmux	
7	Clkdiv8	Main clock divided by 8	7	seqrstb	

Data stream output

clkrateout	dualchannelout	Config.	Description	
0	0	0	The data are sampled by the frequency output clock 40 MHz.	The data stream is output on data line 1 only, Data line 0 stay to low level
0	1	1		The data stream is output on both data line 0 and 1.
1	0	2	The data are sampled by the frequency output clock 80 MHz.	The data stream is output on data line 1 only, Data line 0 stay to low level
1	1	3		The data stream is output on both data line 0 and 1.

2.3.13 RO_MODE0 Register

The RO_MODE0 registers are 8 bits large; they allow the user to select specific digital mode of the chip.

Bit #	Bit Name	Purpose	Basic configuration value	
7	EnVDiscriTestDigital	Enable the internal injection of VTEST	0	External injection of VTEST
6	En_HalfMatrx	Set the row shift register to 320 in place of 576 bits.	0	Normal mode, 576 row shift register selected
5	DisLVDS	Disable LVDS and active clock CMOS.	0	LVDS selected
4	En_LineMarker	Add two rows at the end of matrix for a chip Readout: The LINEPAT_REG register is selected to emulate discriminators outputs. For analogue outputs, the 2 Test Levels, VTEST1 and VTEST2 are selected which emulate a pixel output.	0	Normal mode
3	MODE_SPEAK	Select Marker signal or Readout Clock for digital and analogue data (MK_CLKA and MK_CLKD pads)	0	Marker signal active
2	Pattern_Only	Test Mode: Select LINEPAT_REG to emulate discriminators outputs	0	Normal mode
1	En_ExtStart	Enable external START input synchronisation (1)	0	Normal mode
0	JTAG_Start	Enable Jtag START input synchronisation (2)	0	

(1) The minimum wide of asynchronous external START signal is 500 ns, and this signal is active at high level.

(2) When En_ExtStart is disabled, it's possible to generate internal START by accessing JTAG_Start bit. JTAG_Start signal is realized by three JTAG access: First step, this bit is set to 0, second step it is set to 1, and at last it is set to 0.

2.3.14 RO_MODE1 Register

The RO_MODE1 registers are 8 bits large; they allow selecting specific analogue mode of the chip.

Bit #	Bit Name	Purpose	Basic configuration value	
7	startframe	Reinitializes the frame counter to 0.	0	
6	EnTestAnalog	Enable analog output	0	
5	EnAnaDriverScan	Enable scan pixel mode	0	
4	DisBufRef	Disable the internal reference	0	Select Internal Buffer
3	EnPll	Enable internal PLL	0	
2	EnDiscriAOP	Enable the Power pulse Amplifier	0	Normal mode

1	EnDiscriPwrSave	Enable the discri power pulse mode	0	Normal mode
0	EnTestDiscri	Enable the discri. test mode	0	Normal mode

2.3.15 BYPASS Register

The Bypass register consists of a single bit scan register. It is selected when its code is loaded in the Instruction register, during some actions on the BSR and when the Instruction register contains an undefined instruction.

3 Running MIMOSA26

The following steps describe how to operate MIMOSA26

3.1 After reset

On RSTB active low signal:

- All BIAS registers are set to the default value, i.e. 0
- DIS_DISC is set to 0, i.e. all columns are selected
- RO_MODE0 is set to 0
- RO_MODE1 is set to 0
- CONTROL_PIX_REG is set to 0
- CONTROL_SUZE_REG is set to 0
- SEQUENCER_PIX_REG is set to 0
- SEQUENCER_SUZE_REG is set to 0
- HEADER_REG is set to 0
- LINE0PAT_REG is set to 0
- LINE1PAT_REG is set to 0
- JTAG state machine is in the Test-Logic-Reset state
- JTAG ID_CODE instruction is selected

Then the bias register has to be loaded. The same for the RO_MODE0, RO_MODE1, CONTROL_PIX_REG, CONTROL_SUZE_REG, SEQUENCER_PIX_REG, LINE0PAT_REG, LINE1PAT_REG, HEADER_REG and DIS_DISC registers if the running conditions differ from defaults. Finally the readout can be performed either in normal mode or in test mode.

3.2 Biasing MIMOSA26

The BIAS_DAC register has to be loaded before operating MIMOSA26.
The 19 DACs constituting this register are built with the same 8 bits DAC current generator which has a 1 µA resolution. Specific interfaces like current mirror for current sourcing or sinking and resistors for voltages, customise each bias output. The following table shows the downloaded codes which set the nominal bias.

Internal DAC Name	Simulation			Resolution	Range	Experimental
	$Code_{16}$ - $Code_{10}$	DacInternal current-µA	Output value			$Code_{16}$ - $Code_{10}$
VKIMO	64-100	100	1 V	10 mV	From 0 up to 2.55 V	
IPIX	32-50	50	50 µA	1 µA	From 0 up to 255 µA	
IDIS2	20-32	32	5 µA	156 nA	From 0 up to 255 µA	
IDIS1	20-32	32	10 µA	312 nA	From 0 up to 255 µA	
VDISREF2	76-118	118	1.18 V	10 mV	From 1 up to 1.5 V	
VDISREF1A	80-128	128	1.18 V	250 µV	From -32 up to 32 mV (1)	
VDISREF1B	80-128	128	1.18 V	250 µV	From -32 up to 32 mV (1)	
VDISREF1C	80-128	128	1.18 V	250 µV	From -32 up to 32 mV (1)	
VDISREF1D	80-128	128	1.18 V	250 µV	From -32 up to 32 mV (1)	
IAnaBUF	32-50	50	500 µA	10 µA	From 0 up to 255 µA	
VTEST2	76-118	118	1.18 V	10 mV	From 1 up to 1.5 V	
VTEST1	80-128	128	1.18 V	250 µV	From -32 up to 32 mV (1)	
ILVDS	20-32	32	7 µA	218 nA	From 0 up to 255 µA	
ILVDSTX	28-40	40	40 µA	1 µA	From 0 up to 255 µA	
IDis2PwrS	A-10	10	100 nA	10 nA	From 0 up to 255 µA	
IDis1PwrS	A-10	10	100 nA	10 nA	From 0 up to 255 µA	
IBufBias	A-10	10	10 µA	1 µA	From 0 up to 255 µA	
IPwrSWBias	A-10	10	10 µA	1 µA	From 0 up to 255 µA	
VDISCLP	64-100	100	2.1 V	10 mV	From 1.2 up to 3.2 V	

(1) Referenced with respect to IVDREF2. The threshold voltage of the discriminators ΔVth is defined as Vref1-Vref2 (Vref1=Vref2+ΔVth).

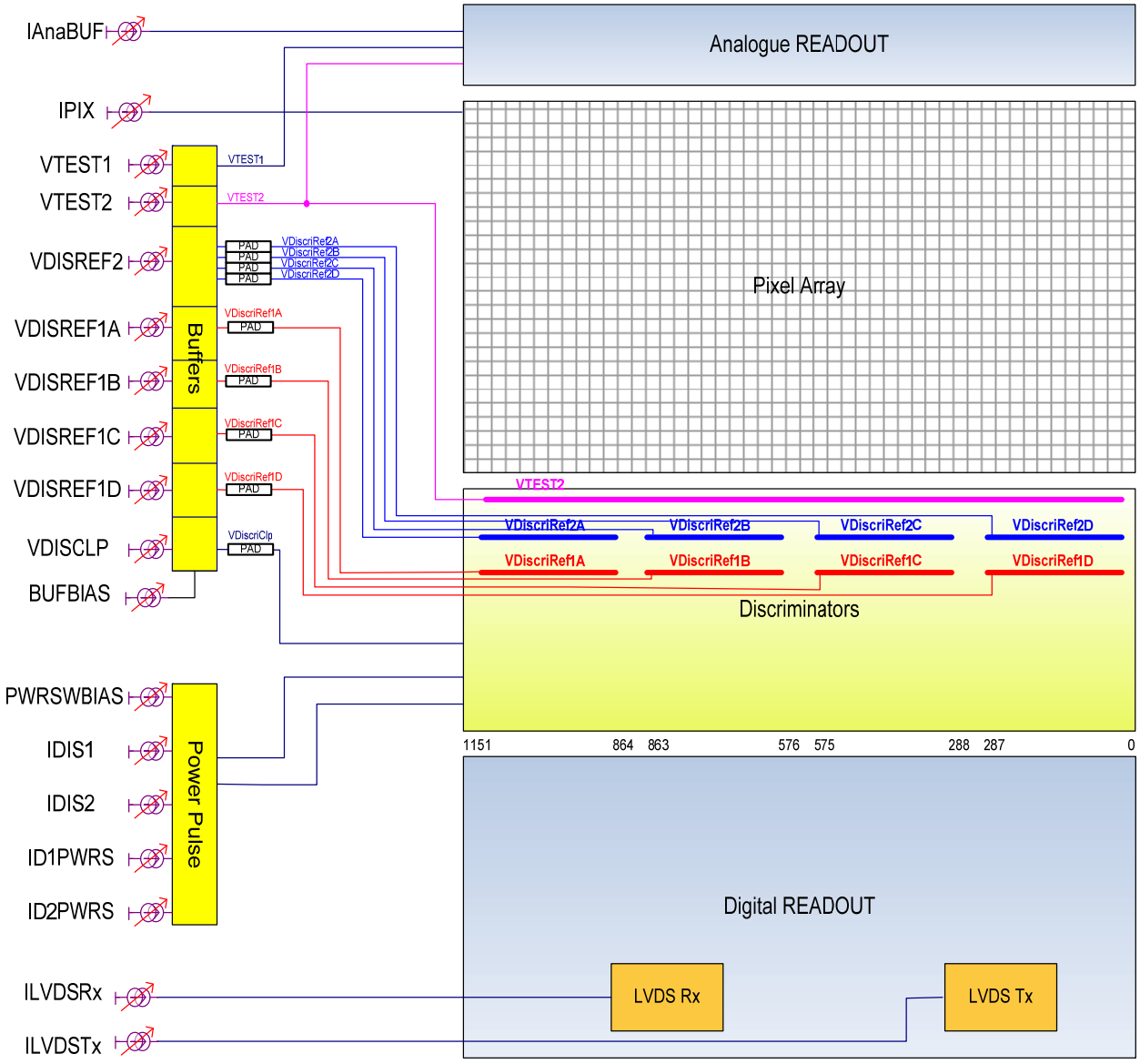


Figure 8: Bias synthetic block diagram

3.3 Setting the Readout Configuration Registers

If the desired operating mode does not correspond to the default one, set LINEPAT0_REG, SEQUENCER_PIX_REG, CONTROL_PIX_REG, LINEPAT1_REG, SEQUENCER_SUZE_REG, HEADER_REG, CONTROL_SUZE_REG, RO_MODE0, RO_MODE1 registers following the §2.3.5, §2.3.7, §2.3.8, §2.3.9, §2.3.10, §2.3.11, §2.3.12, §2.3.13, §2.3.14.

3.4 Readout

3.4.1 Signal protocol

After JTAG registers have been loaded, the readout of MIMOSA26 can be initialized with following signal protocol:

- Start readout clock (CLKL);
- Set SPEAK signal to 0;
- Set START signal to 1 during 500 ns (minimum).The internal reset is created after 2 rising edge of CLKL. After this reset, CkDiv16 (input clock with 1/16 ratio) is generated;

- The readout controller starts at the first falling edge of CkDiv16 after START set to 0.

Signal markers allow the readout monitoring and the data outputs (analogue and digital) sampling:

- CLKA, CLKD and MKD are running when readout controller starts. CLKA is signal which is generated by logic OR between Read and Calib signals.

- When SPEAK signal is active, marker of synchronisation for analogue outputs is generated on MKA pad.

- Marker of synchronisation for digital outputs is generated on MKD pad, this signal is shifted of 4 rising edge of CLKL to *debuttrame* signal, MKD is set during 4 clock's rising edges of CLKD and is not depended of signal SPEAK.

3.4.2 Successive frames and resynchronisation

Successive pixel frames are read until the readout clock is stopped.
A frame resynchronisation can be performed at any time by setting up the "START" token again.

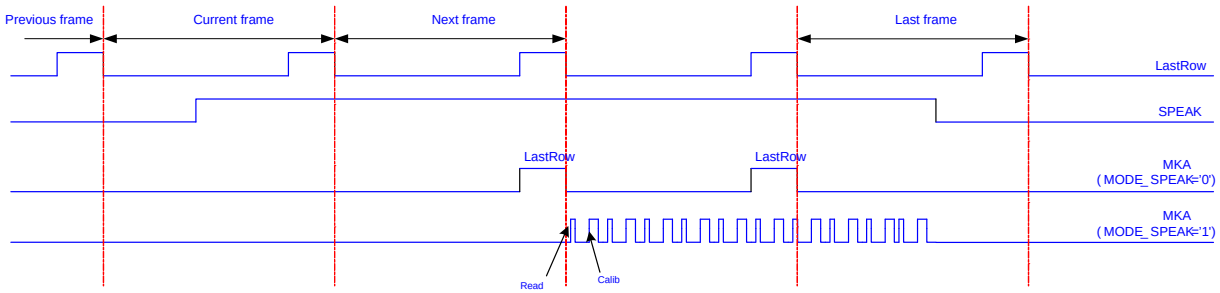


Figure 9: Successive frames and resynchronization timing diagram

SPEAK signal allows to generate markers signals which are used by DAQ. When SPEAK signal is set to 1 during the current frame, analogue marker appears on MKA pad during next frame.
In the MODE_SPEAK='0', the MKA marker corresponds to last row of the frame.
In the MODE_SPEAK='1', MKA signal corresponds to a sampling clock for analogue outputs data (same as CLKA) which starts at the first row of frame. When SPEAK signal is set to 0, MKA is set to 0.

3.5 Analogue and digital Data Format

Two Types of signal can be generated on analogue outputs:

- Normal pixel signal
- Test signal

In concern to digital outputs, two types of signal can be generated:

- Digital pixel signal after zero suppression processing
- Test discriminator and test zero suppression logic:
  - Digital pixel signal by discriminator
  - Test pattern used by zero suppression logic, read to LINEPAT_REG register

MIMOSA26 uses the pads at the bottom edge for all its operations, whatever is collecting data from the pixels (using the pixels and the discriminators) or in test mode (reproducing at the outputs the pre-programmed patterns). All the digital signals for the synchronization and the programming of the chip are necessary for successful operation.
Analog outputs located on the top edge of the chip are not used for the normal operations. The main purpose is the characterization of the pixels or the checking of the dead pixels. Therefore measurements on these pads deal with normal pixel signals as well as test signals (but they still require the synchronization and the markers) and it is activated on demand by setting to 1 the *EnTestAnalog* bit in the RO_MODE1 register.

3.5.1 Normal mode data format

3.5.1.1 Introduction

This chip is the combination between MIMOSA 22 and SUZE 1. The inputs are the main clock, the reset and an input synchronization (START) for initializing the readout control.

The output data of the last frame are sparsified and are sent during the acquisition of the current frame.

The outputs serializing the data of SUZE 1 with the same number of pads of MIMOSA 22 include:

- A clock (CLKD),
- Two data lines (DO0 and DO1), and
- A marker (MKD).

The serial output has four configuration modes according to 2 registers *clkrate* and *dualchannel* (see §2.3.12). as shown later. **All the words (16 bits) are read from the LSB to the MSB**.

The different part of the data frame is the *Header*, *Frame counter*, *Data Length*, *States/Line*, *State*, and *Trailer*.

The 2 words elements (ie *Header*, *Frame counter*, *Data Length* and *Trailer)* are divided into two parts. For instance, the header includes Header0 (corresponds to the 16 bits LSB) and header1 (corresponds to the 16 bits MSB).

The *Header*, the *Trailer* and the *Marker* signal could be used together to detect lose of synchronization.

3.5.1.2 The Clock

The clock is always present even if the data transmission is finished. Its rate depends on the clkrate register. 80 MHz or 40 MHz

3.5.1.3 Marker

The marker (MKD) is available in all modes. The *Marker* signal is set during 4 clock's rising edges and may also be used to detect the beginning of a data transmission.

3.5.1.4 Header trailer

The *Header* and the *Trailer* are composed of 2 x 16 bits (header0 –header1),(trailer0 –trailer1) and allows detecting the beginning and the end of a data transmission. The *Header* and the *Trailer* are totally configurable by JTAG (the header and the trailer of each data frame can be different). The Table 1 (see §2.3.11) shows the possible *Header* and *Trailer* values.

3.5.1.5 Frame counter

Frame counter is the number of frame since the chip was reset. This counter (32 bits) is reset to 0 when the maximum is reached (FFFFFFFF in hexadecimal) and continues to work.

The *Frame counter* when separated into 2 words is given in the *Data line 0* (*Frame counter 0*) with the LSB's and in the *Data line 1* (*Frame counter 1*) the MSB's.

3.5.1.6 Data Length

Data Length is the number of word of 16 bits of the useful data. *Data Length* is written on 32 bits. In the case of one data line, the number of words is repeated 2 times. The sum determines the real value of the useful data

In the case of no hit during a frame, *Data Length 0* and *Data Length 1* are set to zero.

3.5.1.7 Useful data (*States/Line, State)*

The useful data is the daisy chain of *States/Line* and *States.*

The maximum number of the useful data bits sends during one frame is (570 words of 16 bits) 9120.

In some rare case, the number of data generated by the suppression of zeros exceeds the maximum bits capable to be sent, thus the data frame will be truncated.

The data are periodically sent at the beginning of each new frame, and the number of bits which could be sent between two headers is variable and depends on the numbers of the words recorded during the last frame.

Each data lines have the same number of bits. Consequently *Data Length 0* and *Data Length 1* are the same.

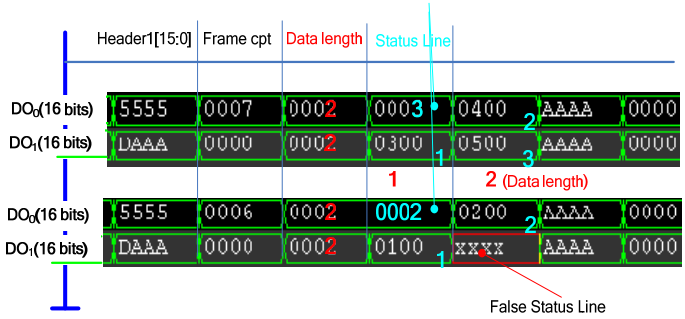
States/Line and *State* have exactly the same meaning whatever the selected mode.

The number of words sent in a data frame depends of the number of hits. If the number of words for the two data lines is odd the last *Status* of *Data line 1* is false. This operating way allows having the same number of bits (Data length) in the both *DO0 and DO1* in every case.

During the treatment of the line, we consider the first word of 16 bits like a status line(n) following of n states, and this operation is done several times until the end of the communication.

We propose to detect this false state (case number of words odd) to count the number of words (of 16 bits) for each new line. If a last word considered like a status line is the last word counted as the total number of words Data Length, then it is a false word that to be ignored.

In the following example the data length is exactly the same but the total number of words can be odd or even.



States/Line contains the address of the line which is hit, the number of *State* for this line (i.e. a number between one and nine), and an overflow flag.

The following table describes the signification of the bits in *Status/Line* word.

Status/ line															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Bit(0-3)				Bit(0-10)											
number of *States*				The address of the line											OVF

Table 2 : Description of *States/line* word

State contains the address of the first hit pixel and the number of successive hit pixels as shown on the table below.

State															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Bit(0-1)		Bit(0-10)													
number of hit pixels		the address of the column											not used		

Table 3 : Description of *State* word

The table below resumes the **maximum** length of the output frame according to the selected mode.

Clk rate out	Dual channel out	Config.	Out	Header	Cptframe	Datalength	Number of useful data (words of 16 bits)	trailer	Total words	Nb of empty words
0	0	0	D00	Unused = 0						
			D01	Header0 & Header1	Cptframe0 & Cptframe1	Datalength0 & Datalength1	278	Trailer0 & Trailer1	286	2
0	1	1	D00	Header0	Cptframe0	Datalength0	282	Trailer0	286	2
			D01	Header1	Cptframe1	Datalength1	282	Trailer1	286	2
1	0	2	D00	Unused = 0						
			D01	Header0 & Header1	Cptframe0 & Cptframe1	Datalength0 & Datalength1	564	Trailer0 & Trailer1	572	4
1	1	3	D00	Header0	Cptframe0	Datalength0	570	Trailer0	574	2
			D01	Header1	Cptframe1	Datalength1	570	Trailer1	574	2

The figure below describes the format of data send by MIMOSA 26 in the one data line mode.

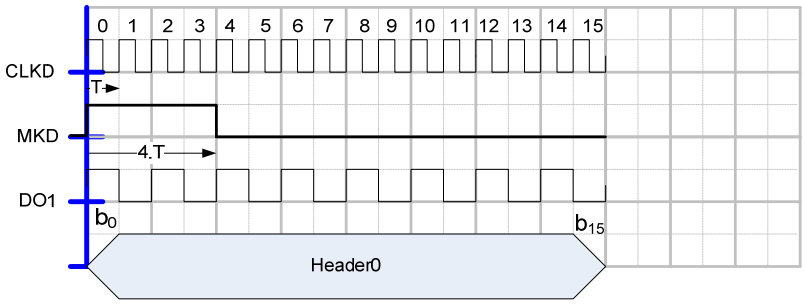


Figure 10: Detail of the beginning of a data frame

Mode 40 MHz Mono channel (*clkrate= 0* and *dualchannel = 0)*

The maximum number of data generated by the suppression of zeros is (278 x 16) bits for the output.
After this overflow, the data frame will be truncated. This mode 0 giving too little information is irrelevant but can be used as test only.

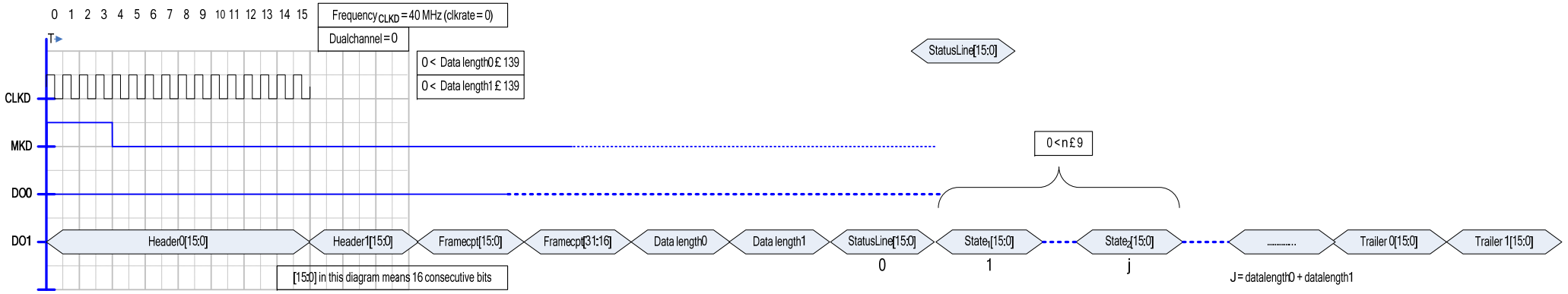


Figure 11: Format of the output Data of MIMOSA 26 Mono Channel and 40 MHz

Mode 40 MHz Dual channel (*clkrate= 0* and *dualchannel = 1)*

The maximum number of data generated by the suppression of zeros is (282 x 16) bits for each output.
After this overflow, the data frame will be truncated.

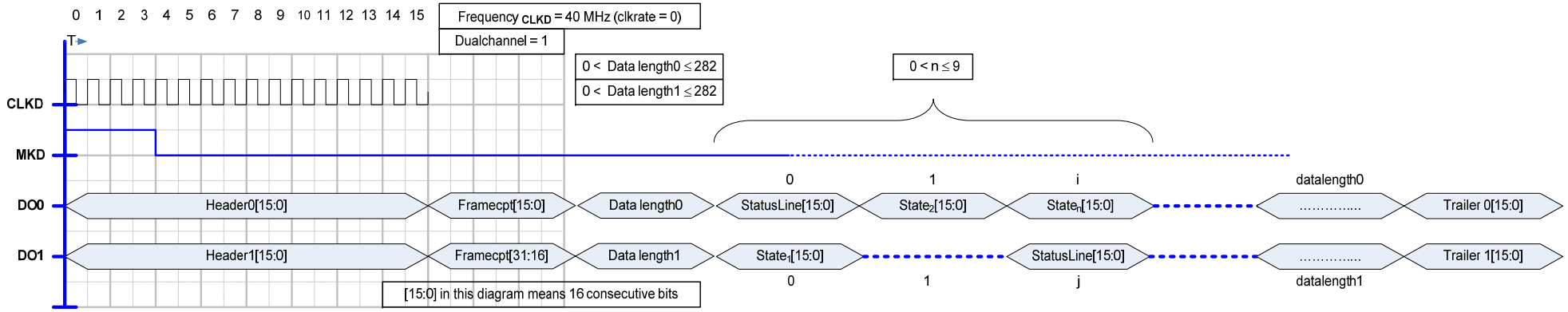


Figure 12: Format of the output Data of MIMOSA 26 Dual Channel and 40 MHz

Mode 80 MHz Mono channel (*clkrate= 1* and *dualchannel = 0)*

The maximum number of data generated by the suppression of zeros is (564 x 16) bits for the output.
After this overflow, the data frame will be truncated.

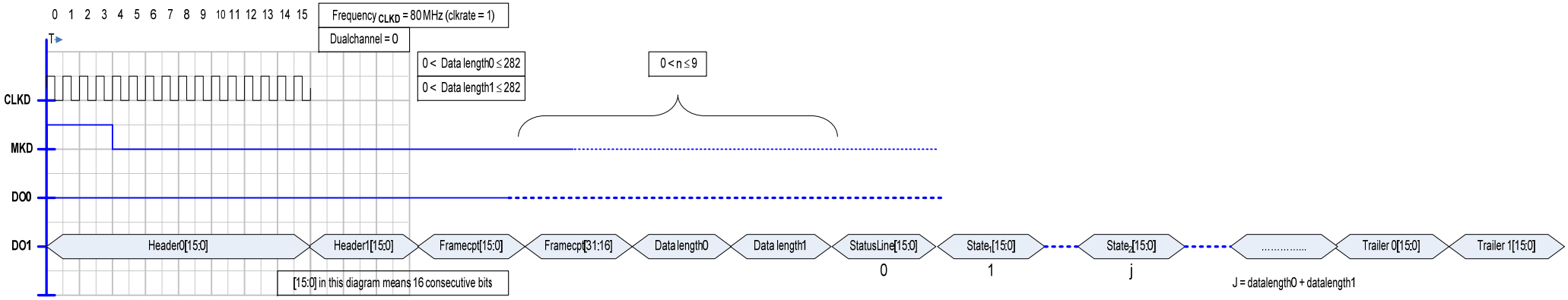


Figure 13: Format of the output Data of MIMOSA 26 Mono Channel and 80 MHz

Mode 80 MHz dualchannel (*clkrate= 1* and *dualchannel = 1)*

The maximum number of data generated by the suppression of zeros is (570 x 16) bits for each output.
After this overflow, the data frame will be truncated.

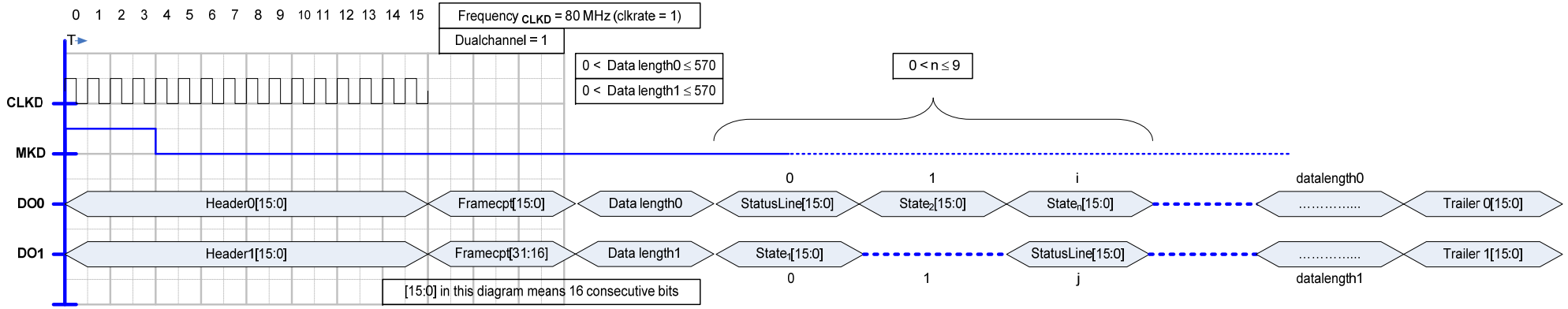


Figure 14: Format of the output data: **Mode 80 MHz dual channel**

3.5.2 Test mode

3.5.2.1 Analogue outputs, Normal pixel signal

When *EnTestAnalog* bit is set to '1' in the RO_MODE1 register, the rightmost 8 columns of pixels are connected to the analog outputs via a voltage follower and the signal is available on the pads. To start the analog test, the *EnAnaDriverScan* must be set to '1' in the RO_MODE1. The scanning of the matrix now starts and stripes of 8 pixels are connected to the analog output. The analog test is performed considering a reduced size of the array (about 576 rows x 8 columns), therefore it takes 144 frame acquisitions to analyze the full matrix. Figure 26 shows how to do the analog characterization and which parts of the matrix are under test for each frame.

The MKA is the synchronization marker for the analog outputs, see When *EnTestAnalog* bit is set to '1' it appears at the end of each frame, this signal is used to sample the analog channel of the new frame on the next raising edge of CLKA. Further when the *EnAnaDriverScan* must be set to '1', this marker appears at the end of the frame for each submatrix.

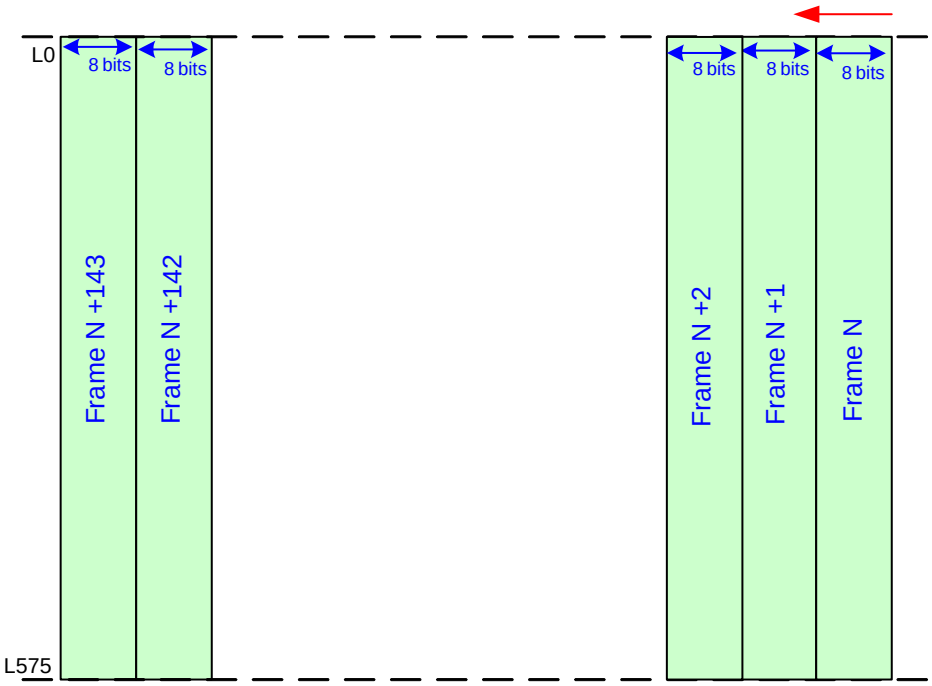


Figure 15: Analog characterization of the pixel

The matrix is divided in stripes of 8 columns and fully scanned at each frame, then swapped with the next block of 8 columns at right and so on until all the columns are analyzed.

Figure 16 – Mode scan for analog output

3.5.2.2 Transfer function of discriminator and pixel digital readout calibration

This test readout mode allows obtaining the transfer function of discriminator and calibrating the digital readout (Pixel + discriminator).

Transfer function of discriminator:

During the test mode (when *EnTestDiscri bit* is set to '1' in the RO_MODE1 register), the pixel matrix is not connected to discriminators. Instead of that, one test level Vtest2 is connected to discriminator input to emulate pixel base line. The Vtest2 voltage can be adjustable via DAC and has to be chosen close to the VDISREF2 voltage. The transfer function is obtained by varying the VDISREF1voltage (A, B, C and D corresponding to the four banks).

Pixel digital readout calibration:

During the test mode (when *EnTestDiscri bit* is set to '0' in the RO_MODE1 register), the pixel is connected to discriminators. This mode allows obtaining pixel digital readout calibration.

During one frame, one row is processed and the outputs of discriminators are serialized with falling edge of CLKD (CLKL/8) and send off chip via DO0 and DO1 pads. The synchronisation marker for digital outputs is generated on MKD pad and corresponding to first bit serialized.

The pixel array calibration can be realized in automatic mode (when *En_auto_scan_discri* is set to 1, §2.3.11). In this mode, the scanning of the pixel array uses 576 frames and stop.

Synoptic

According to the synoptic, the whole line (1152 bits) is scanned and given to two shift register of 576 bits wide.

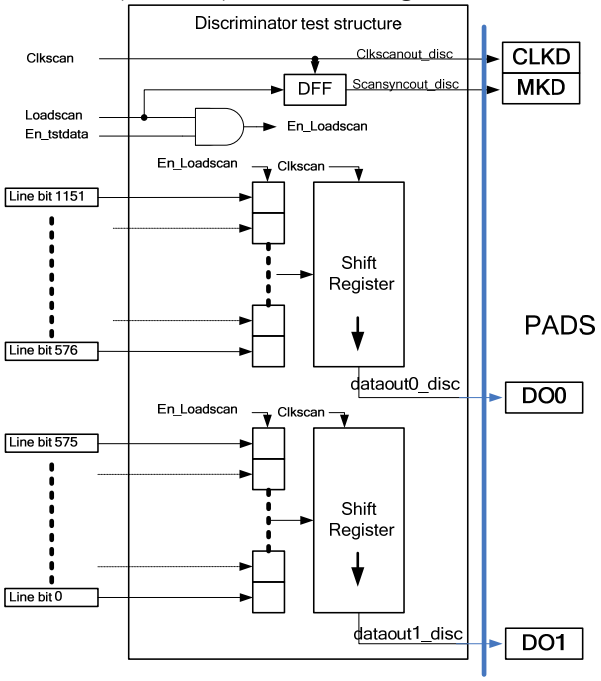


Figure 17: discriminator test block diagram

Timing diagram

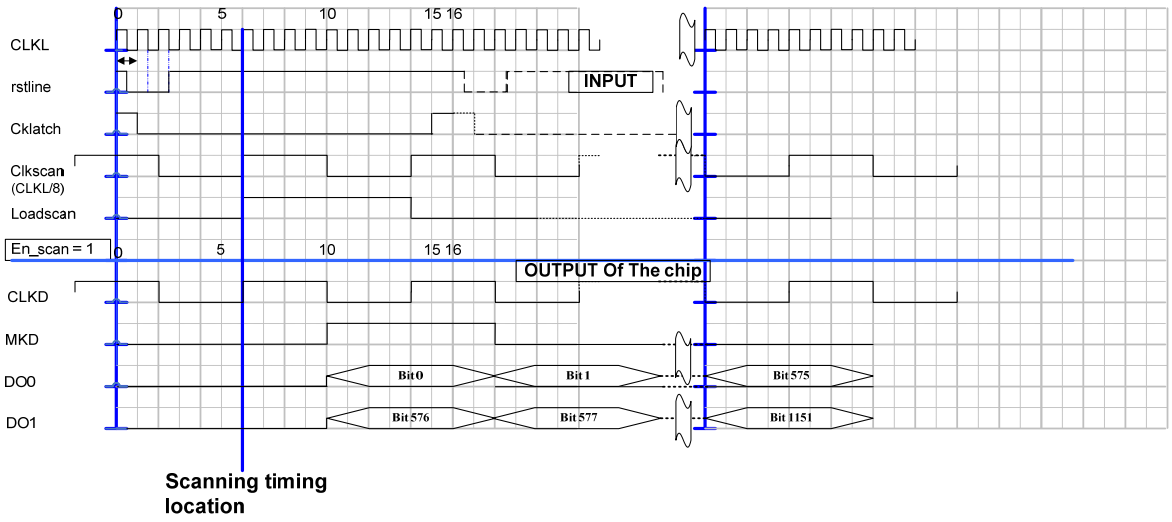


Figure 18: timing diagram Sequence of the line reading

The SCANLINETST of the CONTROL_SUZE_REG Register gives the row address into the frame.

For both modes, the following bits of the CONTROL_SUZE_REG registers are set:

Bit Name	Value configuration
En_scan	1
Test_after_mux	0
entestdatadisc	1

Two modes are defined:

- When En_auto_scan_discri is set to 0, we select one row defined into SCANLINETST(0 to 23F). When this mode is started, at each frame, the selected row is scanned (the readout process is continuous). To change the row address, we define other scan line into SCANLINETST and generate a new START signal.
- When En_auto_scan_discri is set to 1, we select the row automatic scanning (from line 0 to 575) and the process stops when last row is scanned (see the Figure below), *but line 0 and line 573 are not scanned.*

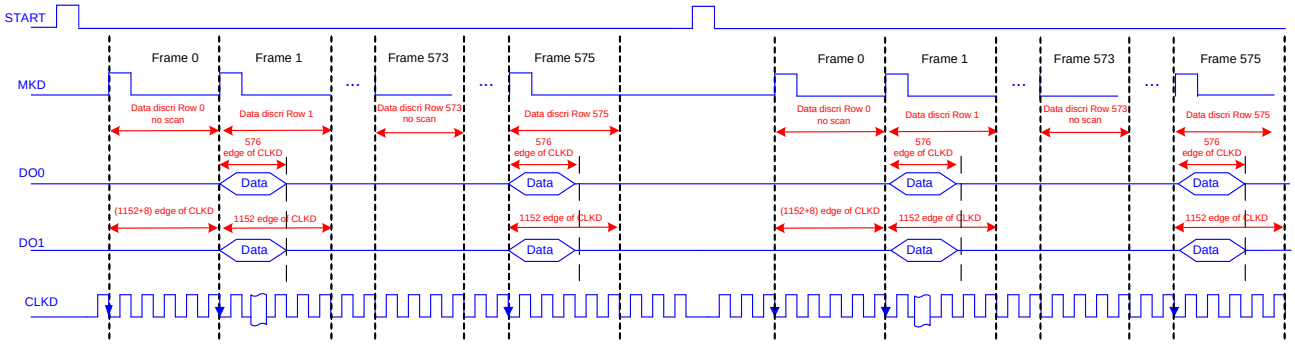


Figure 19: scanning automatic test of the Data discriminator (En_auto_scan_discri = 1)

3.5.2.3 PLA test structure

The mode is reserved for IPHC group.

3.5.2.4 SUZE multiplexer test

The mode is reserved for IPHC group.

3.6 MIMOSA26 Chronograms

The following chronograms describe typical access to the chip; Reset, JTAG download sequence and then the readout.

3.6.1 Normal Readout

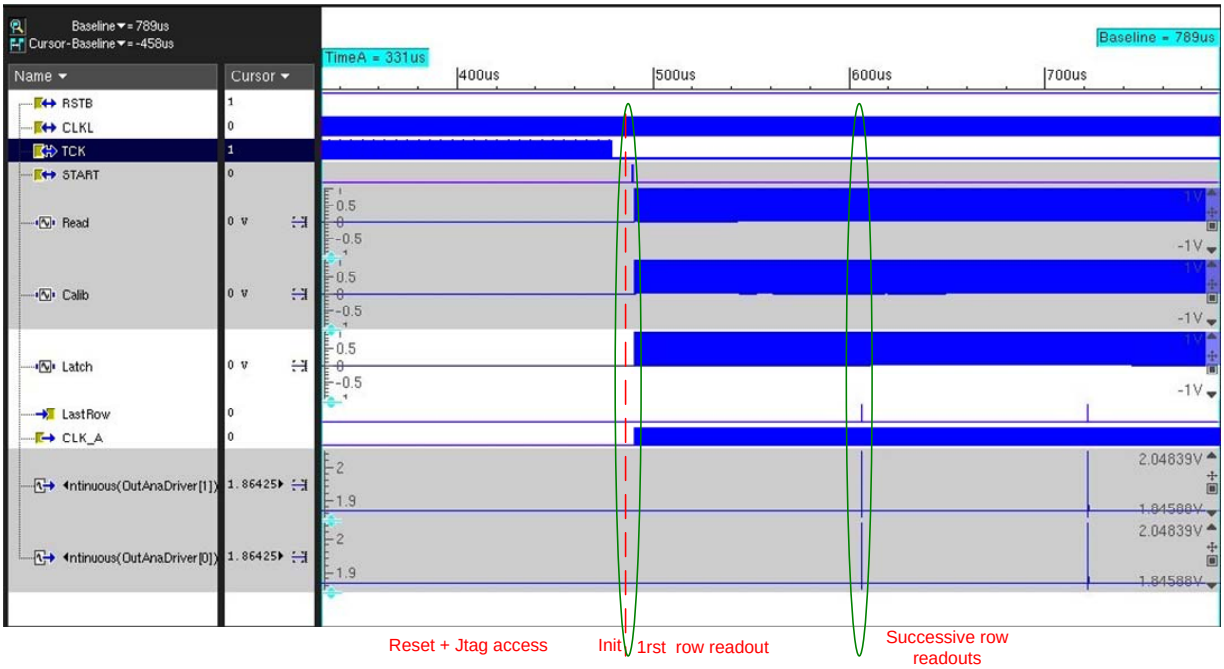


Figure 20: Data readout mode simulation timing diagram

This figure shows the beginning of typical data readout mode. After Reset and JTAG setting, one can see the initialisation phase of the readout of the first pixel row.

3.6.2 Readout synchronisation

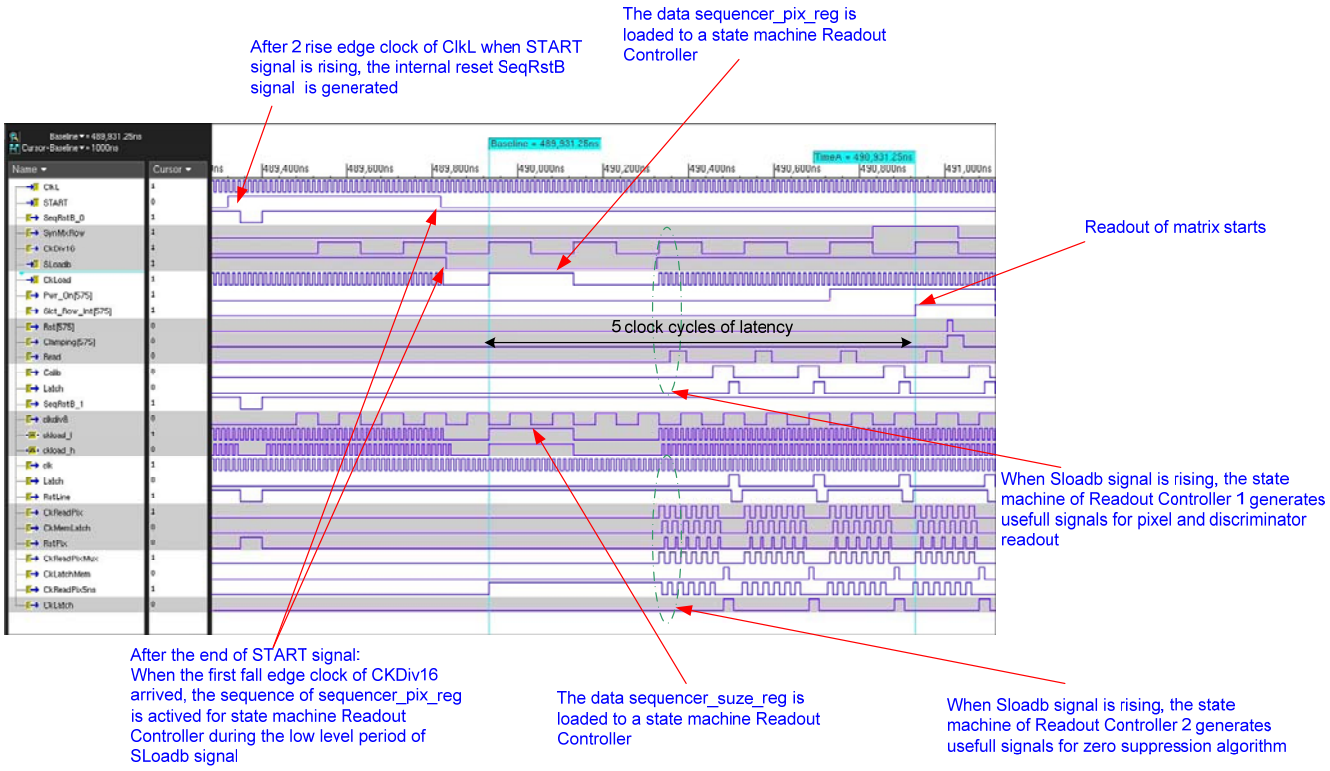

After 2 rise edge clock of ClkL when START signal is rising, the internal reset SeqRstB signal is generated
The data sequencer_pix_reg is loaded to a state machine Readout Controller
Readout of matrix starts
5 clock cycles of latency
When Sloadb signal is rising, the state machine of Readout Controller 1 generates usefull signals for pixel and discriminator readout
After the end of START signal:
When the first fall edge clock of CKDiv16 arrived, the sequence of sequencer_pix_reg is actived for state machine Readout Controller during the low level period of SLoadb signal
The data sequencer_suze_reg is loaded to a state machine Readout Controller
When Sloadb signal is rising, the state machine of Readout Controller 2 generates usefull signals for zero suppression algorithm

Figure 21: zoom on the readout start simulation timing diagram

After a latency of 5 CkDiv16 cycles, readout of matrix starts.

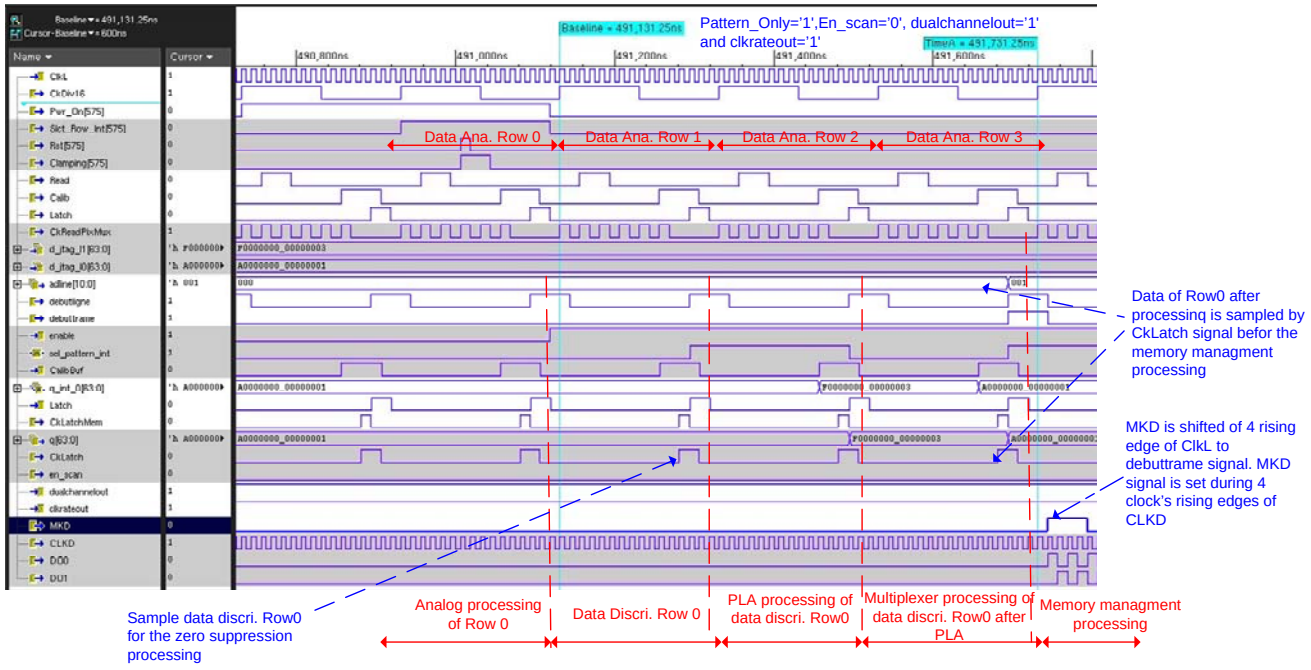

Pattern_Only='1',En_scan='0', dualchannelout='1' and clkrateout='1'
Data Ana. Row 0
Data Ana. Row 1
Data Ana. Row 2
Data Ana. Row 3
Data of Row0 after processinq is sampled by CkLatch signal befor the memory managment processing
MKD is shifted of 4 rising edge of ClkL to debuttrame signal. MKD signal is set during 4 clock's rising edges of CLKD
Sample data discri. Row0 for the zero suppression processing
Analog processing of Row 0
Data Discri. Row 0
PLA processing of data discri. Row0
Multiplexer processing of data discri. Row0 after PLA
Memory managment processing

Figure 22: Pipeline of the readout processing from analog to memory part simulation timing diagram

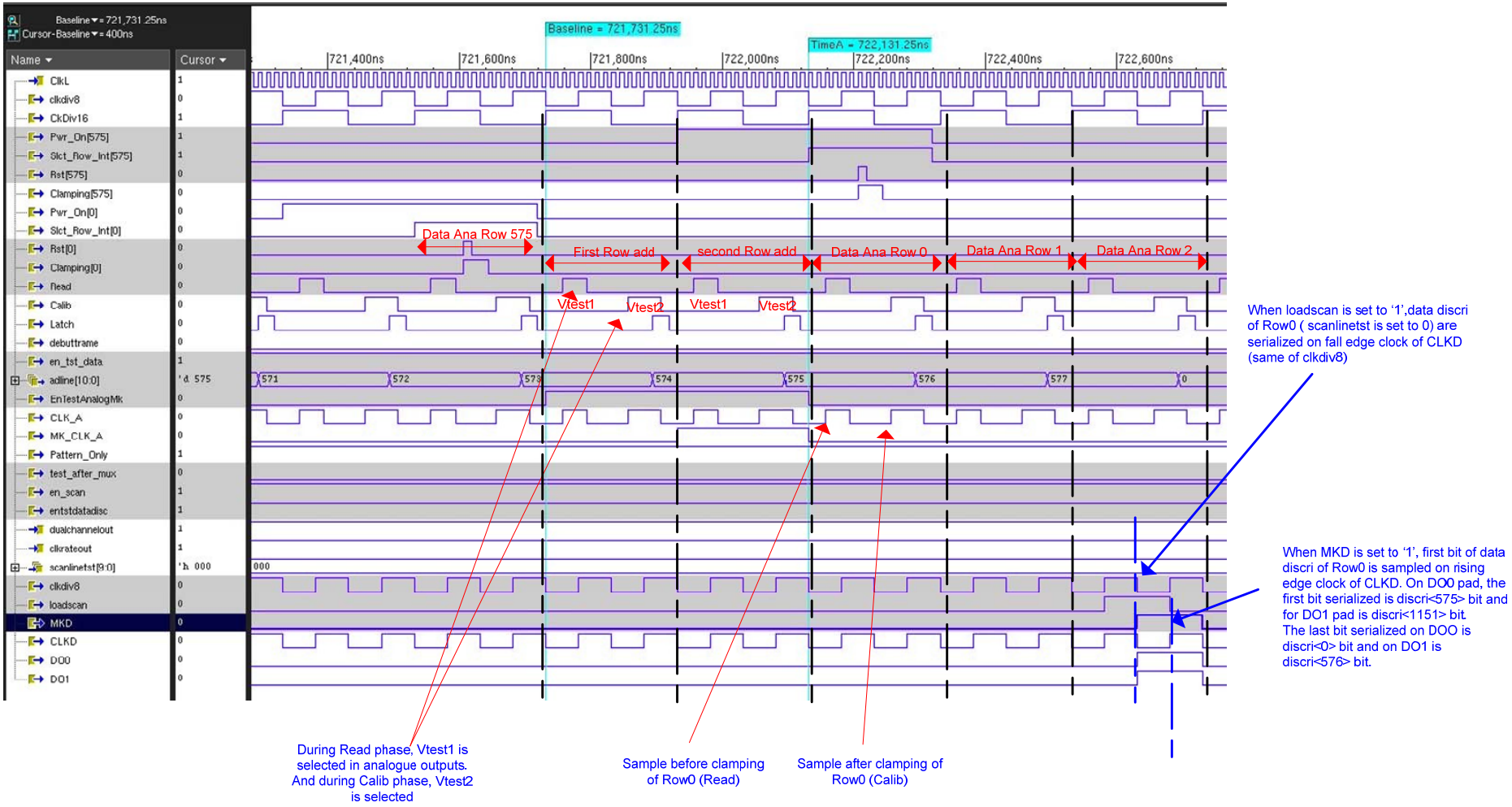

Baseline = 721,731.25ns
TimeA = 722,131.25ns
Data Ana Row 575
First Row add
second Row add
Data Ana Row 0
Data Ana Row 1
Data Ana Row 2
Vtest1
Vtest2
Vtest1
Vtest2
When loadscan is set to '1',data discri of Row0 (scanlinetst is set to 0) are serialized on fall edge clock of CLKD (same of clkdiv8)
When MKD is set to '1', first bit of data discri of Row0 is sampled on rising edge clock of CLKD. On DO0 pad, the first bit serialized is discri<575> bit and for DO1 pad is discri<1151> bit.
The last bit serialized on DOO is discri<0> bit and on DO1 is discri<576> bit.
During Read phase, Vtest1 is selected in analogue outputs. And during Calib phase, Vtest2 is selected
Sample before clamping of Row0 (Read)
Sample after clamping of Row0 (Calib)

Figure 23: Test of the discriminator (1/2)

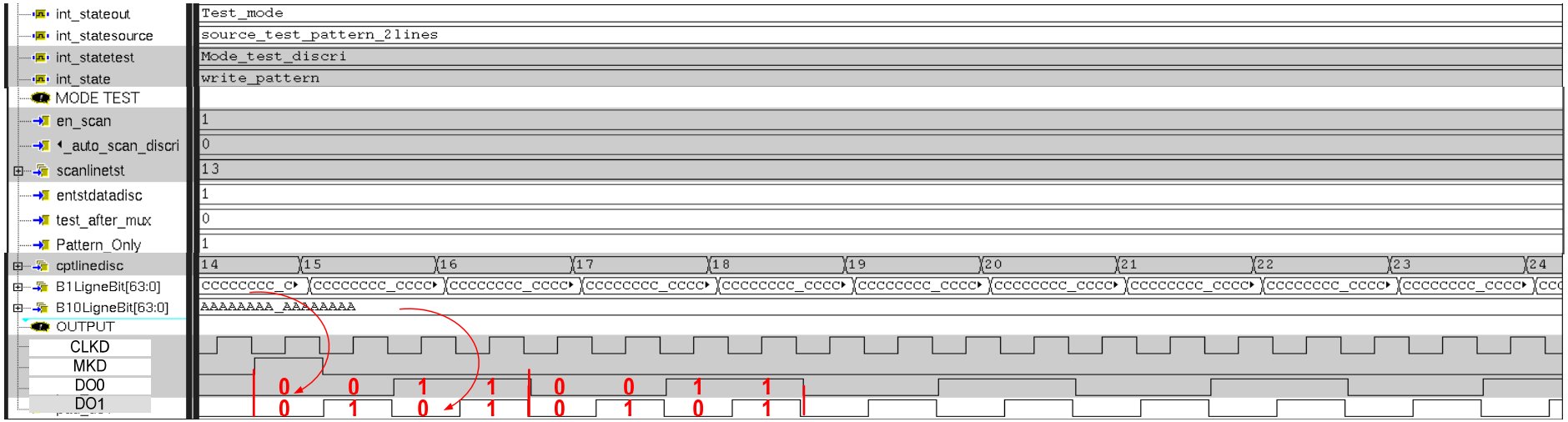


Figure 24: Test of the discriminator (2/2)

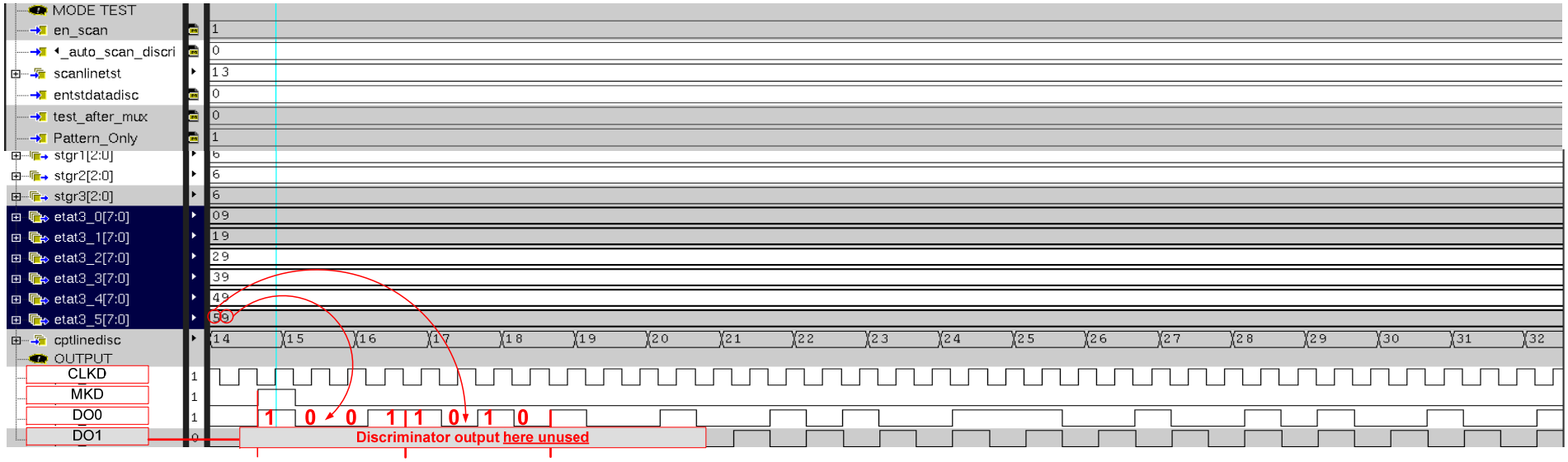


Figure 25: Test of the PLA

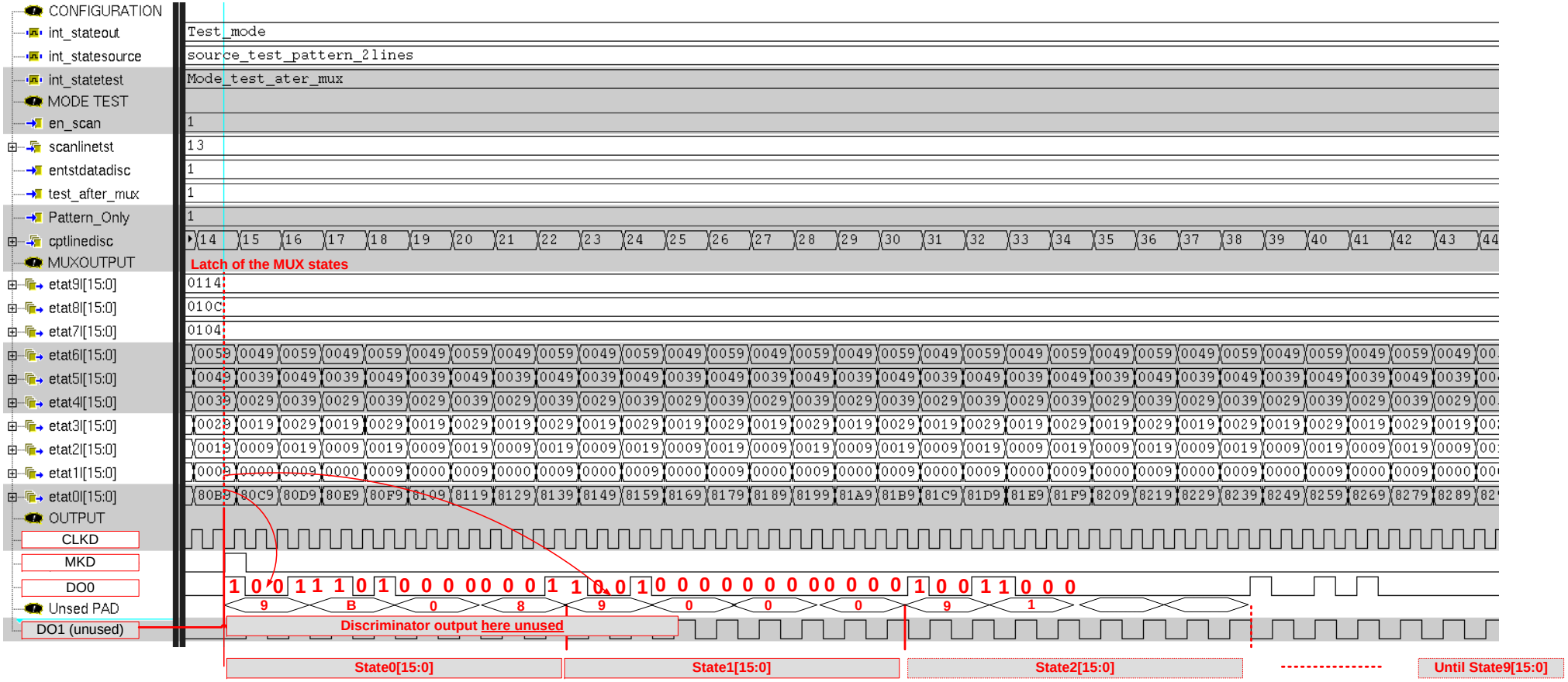


Figure 26: Test of the MUX

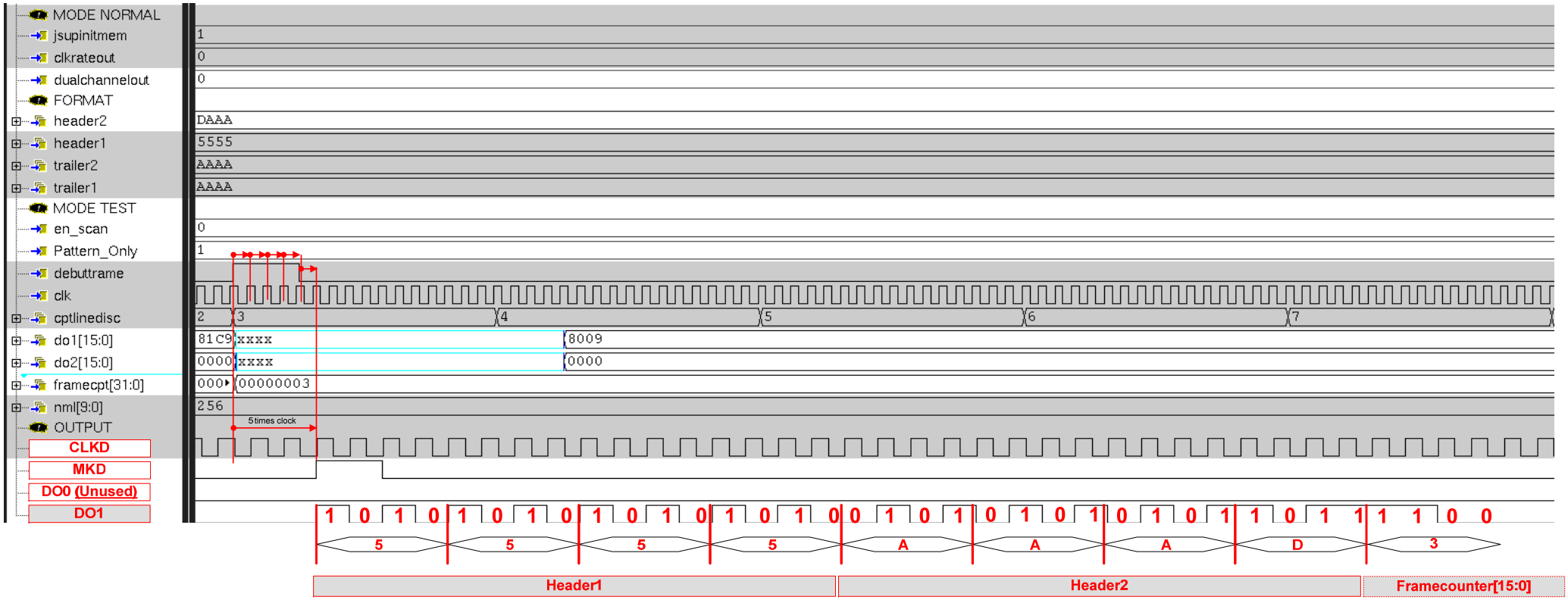


Figure 27: Normal working mode: Clkrate = 0 Dualchannel = 0

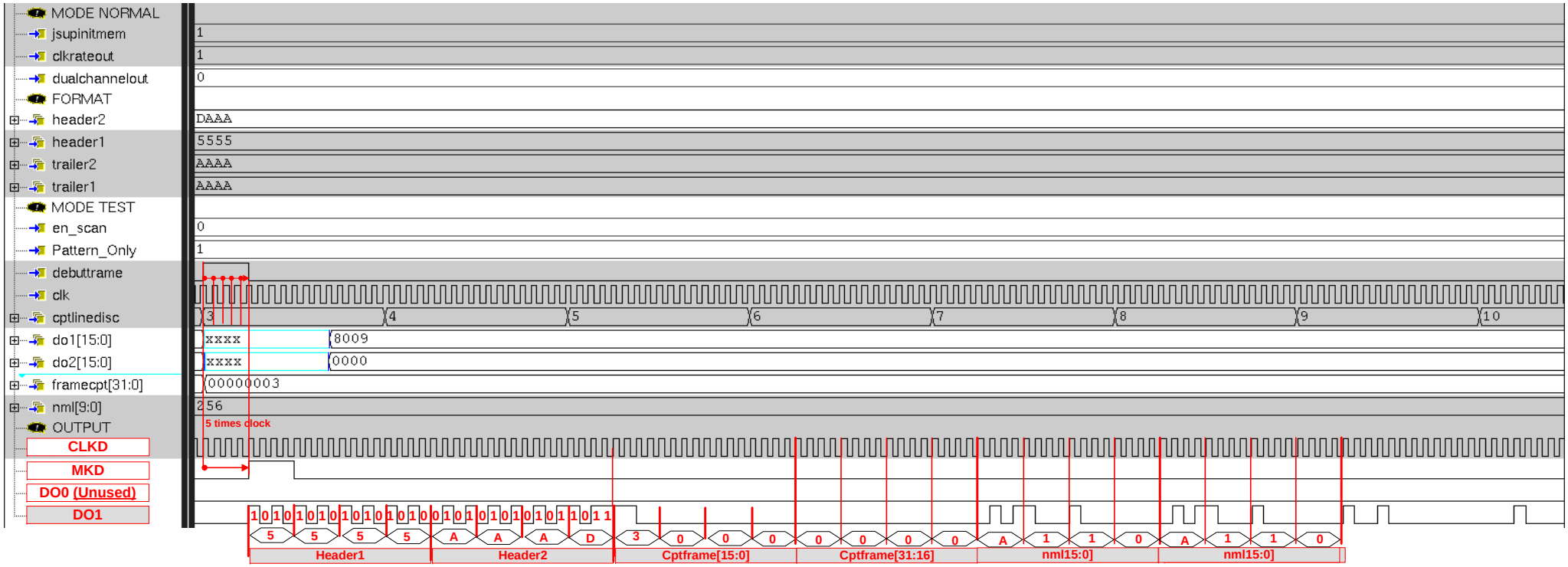


Figure 28: Normal working mode: Clkrate = 1 Dualchannel = 0

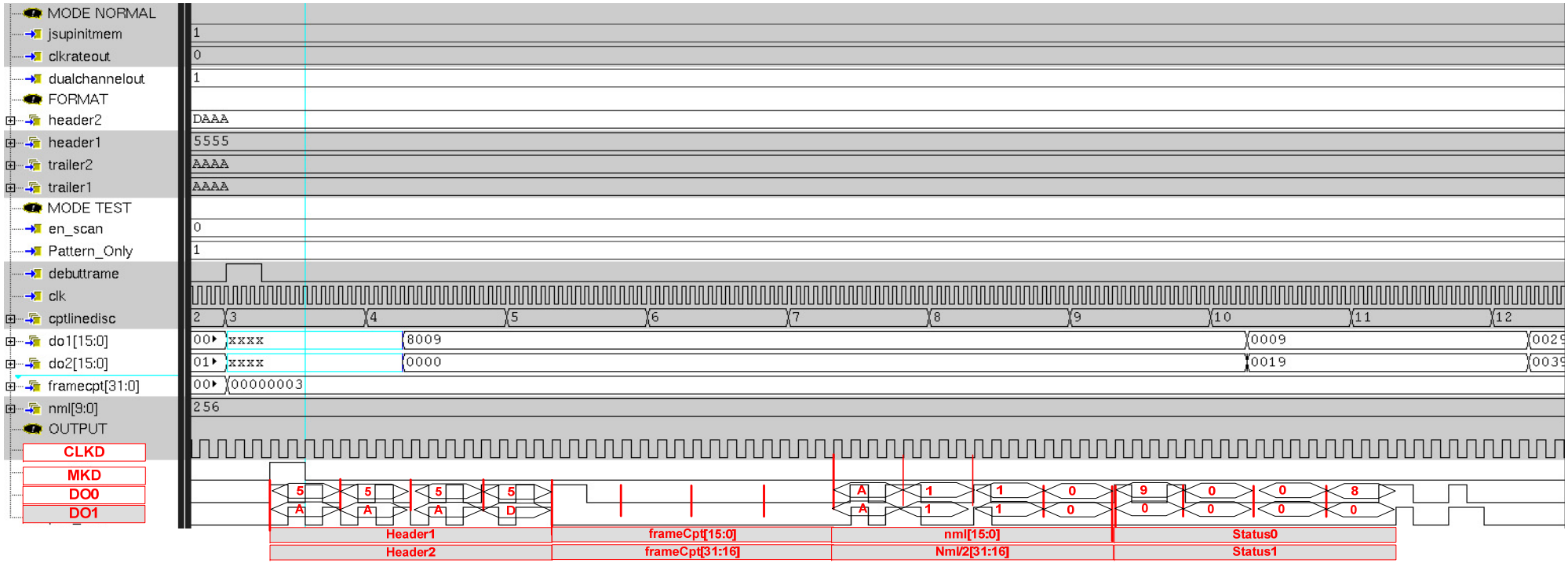


Figure 29: Normal working mode: Clkrate = 0 Dualchannel = 1

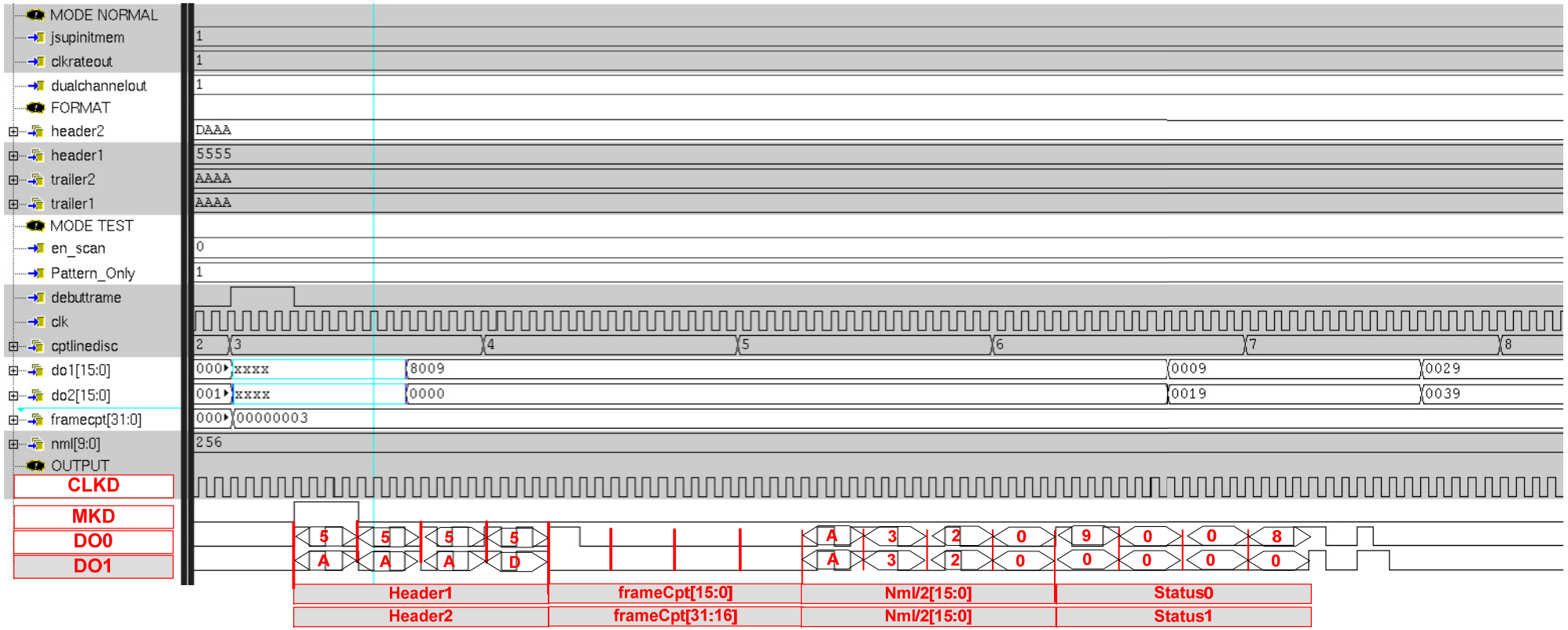


Figure 30: Normal working mode: Clkrate = 1 Dualchannel = 1

3.6.3 Main Signal Specifications

	Parameter	Typical Value	Notes
INIT	RSTB Pulse Width	>1 µS	Active Low, Asynchronous Power on Reset
JTAG	TCK Frequency	10 MHz	Boundary Scan Clock
	TMS Setup/Hold Time	~10 nS	Boundary Scan Control Signal
	TDI Setup/Hold Time	~10 nS	Boundary Scan Serial Data In
READOUT	CKRD Frequency	Up to 80 MHz	Readout Clock LVDS signal
	CKRD Duty Cycle	50%	
	SYNC Setup/Hold Time	5 nS	Chip Initialisation, CMOS signal. Starts after falling edge on 1rst CKRD sampling
Differential Current Buffer (1)	Input Dynamic range	0.7 up to 1.2 V	
	Rise time	5 nS	@ 10-90%, for fully input dynamic range Simulated with Z_{load} = 2*100 Ohm and 2*5pF
	Fall time	5 nS	
	Bandwidth	200 MHz	@ -3 dB
	Transconductance gain	5.8 mS	
	Output Current Range	-2.2; 2.2 mA	
Analogue Driver	Input Dynamic range		
	Rise time		
	Fall time		
	Bandwidth		
	Output Current Range		

Note 1: The differential current output buffer can be modeled as an ideal current source. Its performances in terms of raising and falling times are limited by its load's time constant (R_{load} x C_{load})

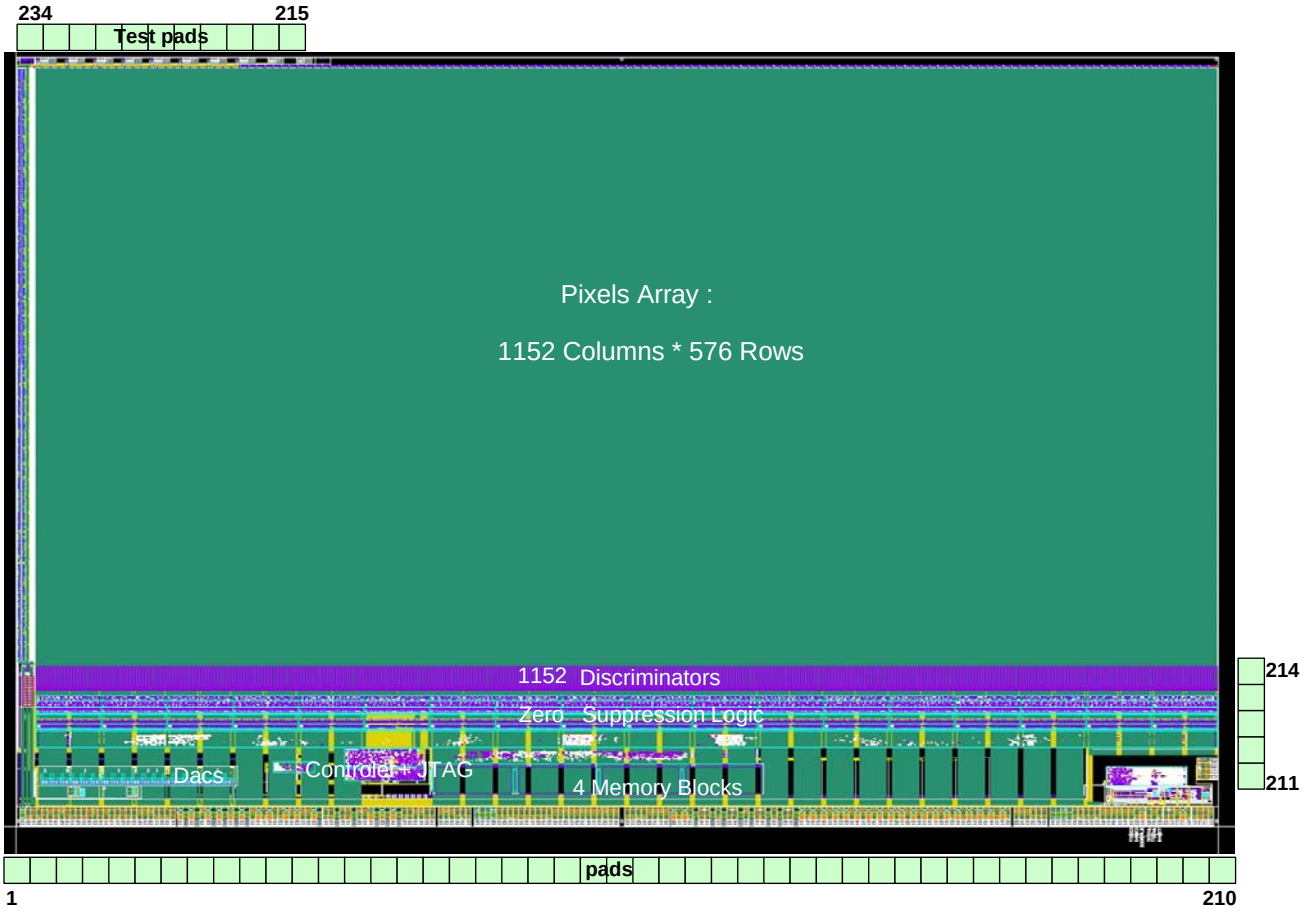
Note 2: Simple source follower

4 Pad Ring

The pad ring of MIMOSA26 is build with

- Pads full custom designed for some of the analogue signals and power supplies
- Pads from the AMS library for the digital signals and power supplies

4.1 MIMOSA26 Pad Ring and Floor Plan View



4.2 Pad List

The bonding of the power supply pads specified in red colour is mandatory

Pad ring segment 1				
Pad	**Name**	**Description**	**Cell**	**Type**
1	TEMP	Temperature sensor	DIRECTPAD	Direct pad
2	gnda	Analogue ground	AGND3ALLP	Power
3	VDiscriRef1A	VDiscriRef1 (Bank A), bidir. test pad (1)	APRIOP	AIO 0 Ohm
4	gnda	Analogue ground	AGND3ALLP	Power
5	VDiscriRef1B	VDiscriRef1 (Bank B), bidir. test pad (1)	APRIOP	AIO 0 Ohm
6	vdda	Analogue power	AVDD3ALLP	Power
7	VDiscriRef1C	VDiscriRef1 (Bank C), bidir. test pad (1)	APRIOP	AIO 0 Ohm
8	vdda	Analogue power	AVDD3ALLP	Power
9	VDiscriRef1D	VDiscriRef1 (Bank D), bidir. test pad (1)	APRIOP	AIO 0 Ohm
10	gnda	Analogue ground	AGND3ALLP	Power
11	VDiscriRef2A	VDiscriRef2 (Bank A), bidir. test pad (1)	APRIOP	AIO 0 Ohm
12	gnda	Analogue ground	AGND3ALLP	Power
13	VDiscriRef2B	VDiscriRef2 (Bank B), bidir. test pad (1)	APRIOP	AIO 0 Ohm
14	vdda	Analogue power	AVDD3ALLP	Power
15	VDiscriRef2C	VDiscriRef2 (Bank C), bidir. test pad (1)	APRIOP	AIO 0 Ohm
16	vdda	Analogue power	AVDD3ALLP	Power
17	VDiscriRef2D	VDiscriRef2 (Bank D), bidir. test pad (1)	APRIOP	AIO 0 Ohm
18	gnda	Analogue ground	AGND3ALLP	Power
19	Vtest	Voltage output of DAC, test pad	APRIOP	AIO 0 Ohm
20	gnda	Analogue ground	AGND3ALLP	Power
21	Itest	Current reference of DAC, test pad	APRIOP	AIO 0 Ohm
22	vdda	Analogue Power	AVDD3ALLP	Power
23	vdda	Analogue Power	AVDD3ALLP	Power
24	vdda	Analogue Power	AVDD3ALLP	Power
25	gnda	Analogue ground	AGND3ALLP	Power
26	gnda	Analogue ground	AGND3ALLP	Power
27	gnda	Analogue ground	AGND3ALLP	Power
28	VDiscriClp	VDiscriClp, bidir. test pad (1)	APRIOP	AIO 0 Ohm
29	CLKA	Readout clock for analogue data	BT4P	DO 3-state, 4 mA
30	Not Connected			
31	MKA	Marker and clock for analogue data	BT4P	DO 3-state, 4 mA
32	Not Connected			
33	vdd	Digital power	AVDD3ALLP	Power
34	TMS	JTAG mode state	ICUP	DI-pullup
35	Not Connected			
36	TDI	JTAG data input	ICUP	DI-pullup
37	Not Connected			
38	TCK	JTAG clock	ICCK2P	DI - clockin
39	Not Connected			
40	TDO	JTAG data output	BT4P	DO 3-state, 4 mA
41	Not Connected			
42	vdd	Digital power	VDD3ALLP	Power
43	Test1Pad	Readout test pad 1	BT2P	DO 3-state, 2mA
44	gnd	Digital ground	GND3ALLP	Power
45	Test2Pad	Readout test pad 2	BT2P	DO 3-state, 2mA
46	gnd	Digital ground	GND3ALLP	Power
47	gnd	Digital ground	GND3ALLP	Power

48	Test3Pad	Readout test pad 3	BT2P	DO 3-state, 2mA
49	vdd	Digital power	VDD3ALLP	Power
50	Test4Pad	Readout test pad 4	BT2P	DO 3-state, 2mA
51	vdd	Digital power	VDD3ALLP	Power
52	vdd	Digital power	VDD3ALLP	Power
53	SPEAK	Active readout marker and clock for analog.	ICPD	DI- pulldown
54	Not Connected			
55	gnd	Digital ground	GND3ALLP	Power
56	gnd	Digital ground	GND3ALLP	Power
57	Not Connected			
58	CLKL_p	Master clock, LVDS compatible	LVDS-RX	DI LVDS
59	CLKL_n	Master clock, LVDS compatible	LVDS-RX	DI LVDS
60	Not Connected			
61	vdd	Digital power	VDD3ALLP	Power
62	vdd	Digital power	VDD3ALLP	Power
63	CLKC	Master clock, CMOS compatible	ICCK2P	DI clockin
64	Not Connected			
65	START	Synchronize the outputs	ICPD	DI- pulldown
66	Not Connected			
67	RSTB	Asynchronous reset, active low	ISUP	DI – pullup, schmitt
68	Not Connected			
69	gnd	Digital ground	GND3ALLP	Power
70	gnd	Digital ground	GND3ALLP	Power
71	vdd	Digital power	VDD3ALLP	Power
72	vdd	Digital power	VDD3ALLP	Power
73	gnd	Digital ground	GND3ALLP	Power
74	gnd	Digital ground	GND3ALLP	Power
75	vdd_latch	Digital latch power	VDD3ALLP	Power
76	vdd_latch	Digital latch power	VDD3ALLP	Power
77	vdd_latch	Digital latch power	VDD3ALLP	Power
78	gnd_latch	Digital latch ground	GND3ALLP	Power
79	gnd_latch	Digital latch ground	GND3ALLP	Power
80	gnd_latch	Digital latch ground	GND3ALLP	Power
81	v_clp	Clamping voltage for pixels	DIRECTPAD	Direct pad
82	v_clp	Clamping voltage for pixels	DIRECTPAD	Direct pad
83	v_clp	Clamping voltage for pixels	DIRECTPAD	Direct pad
84	v_clp	Clamping voltage for pixels	DIRECTPAD	Direct pad
85	gnda	Analogue ground	AGND3ALLP	Power
86	gnda	Analogue ground	AGND3ALLP	Power
87	gnda	Analogue ground	AGND3ALLP	Power
88	gnda	Analogue ground	AGND3ALLP	Power
89	gnda	Analogue ground	AGND3ALLP	Power
90	gnda	Analogue ground	AGND3ALLP	Power
91	gnda	Analogue ground	AGND3ALLP	Power
92	gnda	Analogue ground	AGND3ALLP	Power
93	gnda	Analogue ground	AGND3ALLP	Power
94	gnda	Analogue ground	AGND3ALLP	Power
95	vdda	Analogue power	AVDD3ALLP	Power
96	vdda	Analogue power	AVDD3ALLP	Power
97	vdda	Analogue power	AVDD3ALLP	Power
98	vdda	Analogue power	AVDD3ALLP	Power
99	vdda	Analogue power	AVDD3ALLP	Power
100	vdda	Analogue power	AVDD3ALLP	Power
101	vdda	Analogue power	AVDD3ALLP	Power
102	vdda	Analogue power	AVDD3ALLP	Power
103	vdda	Analogue power	AVDD3ALLP	Power
104	vdda	Analogue power	AVDD3ALLP	Power

105	vdda	Analogue power	AVDD3ALLP	Power
106	vdda	Analogue power	AVDD3ALLP	Power
107	gnd_mem	Digital memory ground	GND3ALLP	Power
108	gnd_mem	Digital memory ground	GND3ALLP	Power
109	gnd_mem	Digital memory ground	GND3ALLP	Power
110	gnd_mem	Digital memory ground	GND3ALLP	Power
111	vdd_mem	Digital memory power	VDD3ALLP	Power
112	vdd_mem	Digital memory power	VDD3ALLP	Power
113	vdd_mem	Digital memory power	VDD3ALLP	Power
114	vdd_mem	Digital memory power	VDD3ALLP	Power
115	WR	Write signal of memory	BT2P	DO 3-state, 2mA
116	gnd	Digital ground	GND3ALLP	Power
117	Fifoinitok	FIFO initialization flag	BT2P	DO 3-state, 2mA
118	gnd	Digital ground	GND3ALLP	Power
119	Not Connected			
120	DO1_n	Data output, channel 1	LVDS-TX	DO LVDS
121	DO1_p	Data output, channel 1	LVDS-TX	DO LVDS
122	Not Connected			
123	gnd	Digital ground	AGND3ALLP	Power
124	Not Connected			
125	DO0_n	Data output, channel 0	LVDS-TX	DO LVDS
126	DO0_p	Data output, channel 0	LVDS-TX	DO LVDS
127	Not Connected			
128	vdd	Digital power	AVDD3ALLP	Power
129	Not Connected			
130	MKD_n	Marker for digital data	LVDS-TX	DO LVDS
131	MKD_p	Marker for digital data	LVDS-TX	DO LVDS
132	Not Connected			
133	gnd	Digital ground	AGND3ALLP	Power
134	Not Connected			
135	CLKD_n	Readout clock for digital data	LVDS-TX	DO LVDS
136	CLKD_p	Readout clock for digital data	LVDS-TX	DO LVDS
137	Not Connected			
138	DataMem<0>	Data bus memory, bit 0	BT2P	DO 3-state, 2mA
139	gnd	Digital ground	AGND3ALLP	Power
140	DataMem<1>	Data bus memory, bit 1	BT2P	DO 3-state, 2mA
141	gnd	Digital ground	AGND3ALLP	Power
142	DataMem<2>	Data bus memory, bit 2	BT2P	DO 3-state, 2mA
143	vdd	Digital power	AVDD3ALLP	Power
144	DataMem<3>	Data bus memory, bit 3	BT2P	DO 3-state, 2mA
145	vdd	Digital power	AVDD3ALLP	Power
146	DataMem<4>	Data bus memory, bit 4	BT2P	DO 3-state, 2mA
147	vdd	Digital power	AVDD3ALLP	Power
148	DataMem<5>	Data bus memory, bit 5	BT2P	DO 3-state, 2mA
149	vdd	Digital power	AVDD3ALLP	Power
150	DataMem<6>	Data bus memory, bit 6	BT2P	DO 3-state, 2mA
151	vdd	Digital power	AVDD3ALLP	Power
152	DataMem<7>	Data bus memory, bit 7	BT2P	DO 3-state, 2mA
153	vdd	Digital power	AVDD3ALLP	Power
154	DataMem<8>	Data bus memory, bit 8	BT2P	DO 3-state, 2mA
155	vdd	Digital power	AVDD3ALLP	Power
156	DataMem<9>	Data bus memory, bit 9	BT2P	DO 3-state, 2mA
157	vdd	Digital power	AVDD3ALLP	Power
158	DataMem<10>	Data bus memory, bit 10	BT2P	DO 3-state, 2mA
159	vdd	Digital power	AVDD3ALLP	Power
160	DataMem<11>	Data bus memory, bit 11	BT2P	DO 3-state, 2mA
161	vdd	Digital power	AVDD3ALLP	Power

162	DataMem<12>	Data bus memory, bit 12	BT2P	DO 3-state, 2mA
163	vdd	Digital power	VDD3ALLP	Power
164	DataMem<13>	Data bus memory, bit 13	BT2P	DO 3-state, 2mA
165	gnd	Digital ground	GND3ALLP	Power
166	DataMem<14>	Data bus memory, bit 14	BT2P	DO 3-state, 2mA
167	gnd	Digital ground	GND3ALLP	Power
168	DataMem<15>	Data bus memory, bit 15	BT2P	DO 3-state, 2mA
169	gnd	Digital ground	GND3ALLP	Power
170	CS	Chip select	BT2P	DO 3-state, 2mA
171	gnd	Digital ground	GND3ALLP	Power
172	selpimp	Internal signal for the test	BT2P	DO 3-state, 2mA
173	gnd	Digital ground	GND3ALLP	Power
174	SYNCHRO	Internal signal, synchro	BT2P	DO 3-state, 2mA
175	gnd	Digital ground	GND3ALLP	Power
176	vdd_latch	Digital latch power	VDD3ALLP	Power
177	vdd_latch	Digital latch power	VDD3ALLP	Power
178	vdd_latch	Digital latch power	VDD3ALLP	Power
179	gnd_latch	Digital latch ground	GND3ALLP	Power
180	gnd_latch	Digital latch ground	GND3ALLP	Power
181	gnd_latch	Digital latch ground	GND3ALLP	Power
182	v_clp	Clamping voltage for pixels	DIRECTPAD	Direct pad
183	v_clp	Clamping voltage for pixels	DIRECTPAD	Direct pad
184	v_clp	Clamping voltage for pixels	DIRECTPAD	Direct pad
185	v_clp	Clamping voltage for pixels	DIRECTPAD	Direct pad
186	gnda	Analogue ground	AGND3ALLP	Power
187	gnda	Analogue ground	AGND3ALLP	Power
188	gnda	Analogue ground	AGND3ALLP	Power
189	gnda	Analogue ground	AGND3ALLP	Power
190	gnda	Analogue ground	AGND3ALLP	Power
191	vdda	Analogue power	AVDD3ALLP	Power
192	vdda	Analogue power	AVDD3ALLP	Power
193	vdda	Analogue power	AVDD3ALLP	Power
194	vdda	Analogue power	AVDD3ALLP	Power
195	vdda	Analogue power	AVDD3ALLP	Power
196	vdd	Digital PLL power	VDD3ALLP	Power
197	gnd	Digital PLL ground	GND3ALLP	Power
198	REFCLK	Clock reference for PLL	ICCK2P	DI clockin
199	gnda	Analogue PLL ground	AGND3ALLP	Power
200	vdda	Analogue PLL power	AVDD3ALLP	Power
201	gnda	Analogue PLL ground	AGND3ALLP	Power
202	Dout_n	Data output of 8b10b	LVDS-TX	DO LVDS
203	Dout_p	Data output of 8b10b	LVDS-TX	DO LVDS
204	vdd	Digital 8b10b power	VDD3ALLP	Power
205	Start_8b10b	Synchronization of 8b10b output	ICP	DI
206	gnd	Digital 8b10b ground	GND3ALLP	Power
207	gnd	Digital 8b10b ground	GND3ALLP	Power
208	BitClock_p	8b10b input clock	LVDS-RX	DI LVDS
209	BitClock_n	8b10b input clock	LVDS-RX	DI LVDS
210	vdd	Digital 8b10b power	VDD3ALLP	Power

Pad ring segment 2				
Pad	**Name**	**Description**	**Cell**	**Type**
211	gnd	Digital LVDS pad ground	GND3ALLP	Power
212	CLKPLL_n	PLL output clock	LVDS-TX	DO LVDS
213	CLKPLL_p	PLL output clock	LVDS-TX	DO LVDS
214	vdd	Digital LVDS pad power	VDD3ALLP	Power

Pad ring segment 3				
Pad	**Name**	**Description**	**Cell**	**Type**
215	Not Connected			
216	gnda	Analogue test mode ground	g_pad	power
217	Not Connected			
218	vdda	Analogue test mode power	g_pad	power
219	Not Connected			
220	OutAnaDriver<0>	Analog output<0> test mode	g_pad	Test pad
221	Not Connected			
222	OutAnaDriver<1>	Analog output<1> test mode	g_pad	Test pad
223	Not Connected			
224	OutAnaDriver<2>	Analog output<2> test mode	g_pad	Test pad
225	Not Connected			
226	OutAnaDriver<3>	Analog output<3> test mode	g_pad	Test pad
227	Not Connected			
228	OutAnaDriver<4>	Analog output<4> test mode	g_pad	Test pad
229	Not Connected			
230	OutAnaDriver<5>	Analog output<5> test mode	g_pad	Test pad
231	Not Connected			
232	OutAnaDriver<6>	Analog output<6> test mode	g_pad	Test pad
233	Not Connected			
234	OutAnaDriver<7>	Analog output<7> test mode	g_pad	Test pad

(1) The buffer could be disable by the bit name DisBufRef in the RO_MODE1 Register (see 2.3.14), consequently the pad can be used as an injection point.

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5 Glossary, Abbreviations and acronyms tables.

Abbreviation or acronym	Meaning	Description
ETU	Elementary Time Unit	$ETU = 1timeclock = \frac{1}{main\_chip\_frequency} = \frac{1}{80MHz} = 12.5ns$
SUZE	Suppression of zeroes	
AD	Address	
D	Data	
TCK	Test clock	Cf. JTAG interface IEEE 1149
TMS	Test Management System	Cf. JTAG interface IEEE 1149
TDI	Test Data Input	Cf. JTAG interface IEEE 1149
TDO	Test Data Output	Cf. JTAG interface IEEE 1149
FIFO		Memory First In first Out,
LVDS		Low voltage differential signalling
PLA	Priority Look Ahead	Asynchronous way to access from a hit to another hit. The next one has the priority
MUX	Multiplexer	Structure that catches only nine groups of pixels among 6 x 18 groups. The first 9 states are kept.
PLA	Priority Look Ahead	Asynchronous way to access from a hit to another hit. The next one has the priority

Word or locution	Description or explanation
Frame	The frame is a set of line, here compound of MaxAdrRow lines.
Line duration	In default mode, 200 ns i.e. 16 times the period of the main clock 80 MHz.(12.5 ns)
Frame duration	= duration line x the content of the cycleMax register.